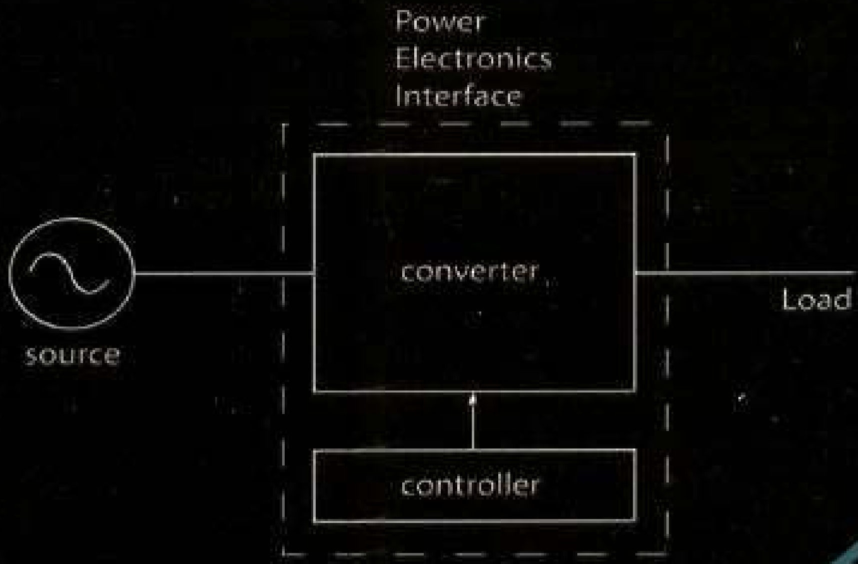
FIRST COURSE ON
POWER ELECTRONICS
AND DRIVES

Year 2003 Edition


Power
Electronics
Interface
converter
source
Load
controller

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First Course on

POWER ELECTRONICS
AND DRIVES

Ned Mohan

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Minneapolis

To my wife Mary, son Michael and daughter Tara

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PREFACE

Power electronics and drives are enabling technologies but most undergraduates, at best, will take only one course in these subjects. Recognizing this reality, this book is intended to teach students both the fundamentals in the context of exciting new applications and the practical design to meet the following objectives simultaneously:

- Provide solid background in fundamentals to prepare students for advanced courses
- Teach design fundamentals so that students can be productive in industry from the very beginning

In this book, the topics listed below are carefully sequenced to maintain student interest throughout the course and to maintain continuity as much as possible.

1. Applications and Structure of Switch-Mode Power Electronics Systems
2. Practical Details of Implementing a Switching Power-Pole (the building block)
3. DC-DC Converters: Switching Details and their Average Dynamic Models
4. Designing the Feedback Controller in DC-DC Converters
5. Diode Rectifiers and their Design
6. Power-Factor-Correction Circuits (PFCs) including the Controller Design
7. Review of Magnetic Concepts
8. Transformer-Isolated Switch-Mode DC Power Supplies
9. Design of High-Frequency Inductors and Transformers
10. Soft-Switching in DC-DC Converters, and its applications in High-Frequency AC Synthesis in Induction Heating and Compact Fluorescent Lamps (CFLs)
11. Electric Motor Drives
12. Synthesis of DC and Low-Frequency Sinusoidal AC in Motor Drives and Uninterruptible Power Supplies (UPS)
13. Control of Electric Drives and UPS
14. Thyristor Converters
15. Utility Applications of Power Electronics

Instructor's Choice

In a fast pace course with proper student background, this book with all these topics can be covered from front-to-back in one semester. However, the material is arranged in such a way that an instructor can either omit an entire topic or cover it quickly to provide just an overview using the PowerPoint-based slides on the accompanying CD, without interrupting the flow.

This book is designed to serve as a semester-course textbook in two different curricula: 1) in a Power Electronics course where there is a separate undergraduate course offered on electric machines and drives, and 2) in a Power Electronics and Drives course where only a single course is offered on both of these subjects. The selections of chapters under these two circumstances are suggested below.

Textbook in a Power Electronics Course. In this course, since a separate undergraduate course exists on electric machines and drives, Chapter 11 on Electric Motor Drives and Chapter 13 on Design of Feedback Controllers in Motor Drives can be omitted. Depending on the availability of time, the "deeper" chapters such as Chapter 6 on Power Factor Control, Chapter 9 on Design of High-Frequency Inductors and Transformers, and Chapter 10 on Soft-Switching Converters can be covered very quickly, mainly to provide an overview.

Textbook in a Power Electronics and Drives Course. Since this course is intended to provide a broader coverage in a single semester by covering topics in power electronics as well in electric drives, some of the "deeper" chapters in power electronics listed earlier can be safely omitted.

Simulations

In Power Electronics, simulations using PSpice can be extremely beneficial for reaffirming the fundamentals and in describing the design details by making realistic problems. However, simulations are presented on the accompanying CD-ROM such that not to get in the way of the fundamentals.

CD-ROM

The accompanying CD includes the following:

- Extremely useful for Instructors: PowerPoint-based slides are included for every chapter to quickly prepare lectures and to review the material in class. Students can print all the slides and bring to the classroom to take notes on.
- Simulations and design examples are ready-to-execute, using PSpice that is loaded on this accompanying CD-ROM.

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Chapter 1

POWER ELECTRONICS AND DRIVES: ENABLING TECHNOLOGIES

1-1 INTRODUCTION TO POWER ELECTRONICS AND DRIVES

Power electronics is an enabling technology, providing the needed interface between the electrical source and the electrical load, as depicted in Fig. 1-1 [1]. The electrical source and the electrical load can, and often do, differ in frequency, voltage amplitudes and the number of phases. The power electronics interface facilitates the transfer of power from the source to the load by converting voltages and currents from one form to another, in which it is possible for the source and load to reverse roles. The controller shown in Fig. 1-1 allows management of the power transfer process in which the conversion of voltages and currents should be achieved with as high energy-efficiency and high power density as possible. Adjustable-speed electric drives represent an important application of power electronics.

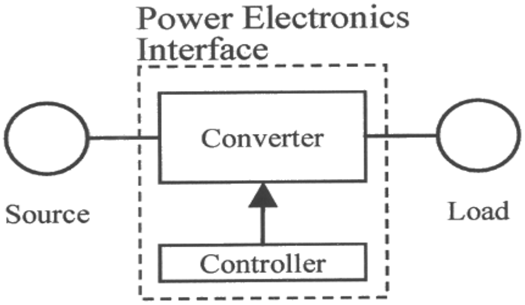


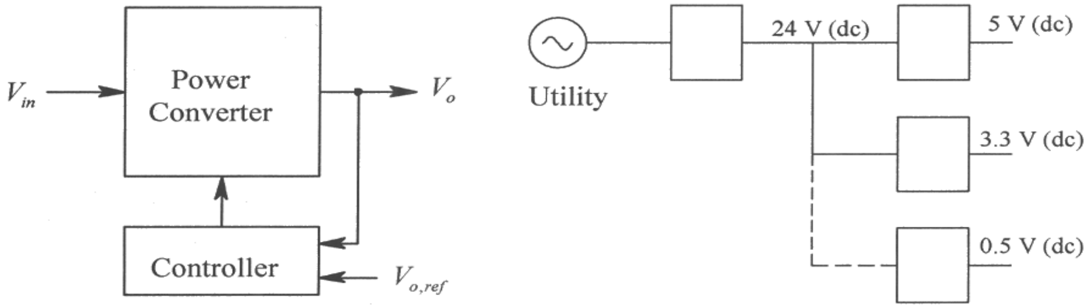
Figure 1-1 Power electronics interface between the source and the load.

1-2 APPLICATIONS AND THE ROLE OF POWER ELECTRONICS AND DRIVES

Power electronics and drives encompass a wide array of applications. A few important applications and their role are described below.

1-2-1 Powering the Information Technology

Most of the consumer electronics equipment such as personal computers (PCs) and entertainment systems supplied from the utility mains internally need very low dc voltages. They, therefore, require power electrics in the form of switch-mode dc power supplies for converting the input line voltage into a regulated low dc voltage, as shown in Fig. 1-2a. Fig. 1-2b shows the distributed architecture typically used in computers in which the incoming ac voltage from the utility is converted into dc voltage, for example, at 24 V. This semi-regulated voltage is distributed within the computer where on-board power supplies in logic-level printed circuit boards convert this 24 V dc input voltage to a lower voltage, for example 5 V dc, which is very tightly regulated. Very large scale integration and higher logic circuitry speed require operating voltages much lower than 5 V, hence 3.3 V, 1 V, and eventually, 0.5 V levels would be needed.



(a) (b)

Figure 1-2 Regulated low-voltage dc power supplies.

Many devices such as cell phones operate from low battery voltages with one or two battery cells as inputs. However, the electronic circuitry within them requires higher voltages thus necessitating a circuit to boost input dc to a higher dc voltage as shown in the block diagram of Fig. 1-3.

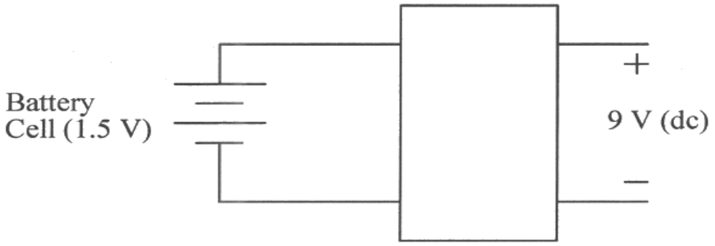


Figure 1-3 Boost dc-dc converter needed in cell operated equipment.

1-2-2 Robotics and Flexible Production

Robotics and flexible production are now essential to industrial competitiveness in a global economy. These applications require adjustable speed drives for precise speed and position control. Fig. 1-4 shows the block diagram of adjustable speed drives in which the ac input from a 1-phase or a 3-phase utility source is at the line frequency of 50 or 60 Hz. The role of the power electronics interface, as a power-processing unit, is to provide the required voltage to the motor. In the case of a dc motor, dc voltage is supplied with adjustable magnitude that controls the motor speed. In case of an ac motor, the power electronics interface provides sinusoidal ac voltages with adjustable amplitude and frequency to control the motor speed. In certain cases, the power electronics interface may be required to allow bi-directional power flow through it, between the utility and the motor-load.

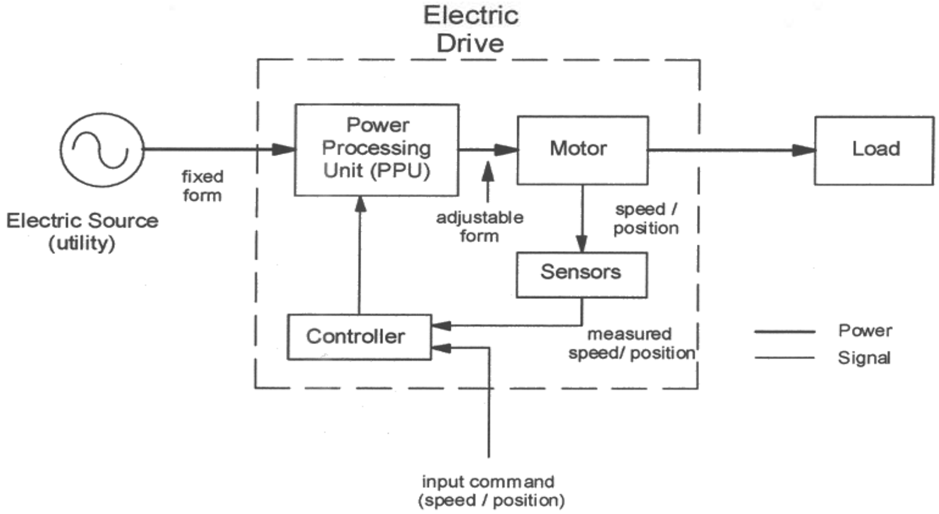

Electric Drive
Electric Source (utility)
fixed form
Power Processing Unit (PPU)
Motor
Load
adjustable form
speed / position
Sensors
Controller
measured speed/ position
input command (speed / position)
Power
Signal

Figure 1-4 Block diagram of adjustable speed drives.

Induction heating and electric welding, shown in Fig. 1-5 and Fig. 1-6 by their block diagrams are other important industrial applications of power electronics for flexible production.

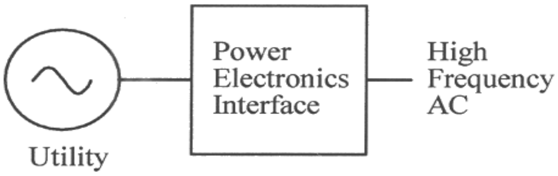

Power Electronics Interface
High Frequency AC
Utility

Figure 1-5 Power electronics interface required for induction heating.

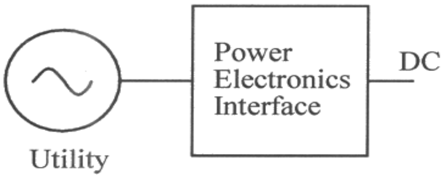

Power Electronics Interface
DC
Utility

Figure 1-6 Power electronics interface required for electric welding.

1-3 ENERGY AND THE ENVIRONMENT

There is a growing body of evidence that burning of fossil fuels causes global warming that may lead to disastrous environmental consequences. Power electronics and drives can play a crucial role in minimizing the use of fossil fuels, as briefly discussed below.

1-3-1 Energy Conservation

It's an old adage: a penny saved is a penny earned. Not only energy conservation leads to financial savings, it helps the environment. The pie chart in Fig. 1-7 shows the percentages of electricity usage in the United States for various applications. The potentials for energy conservation in these applications are discussed below.

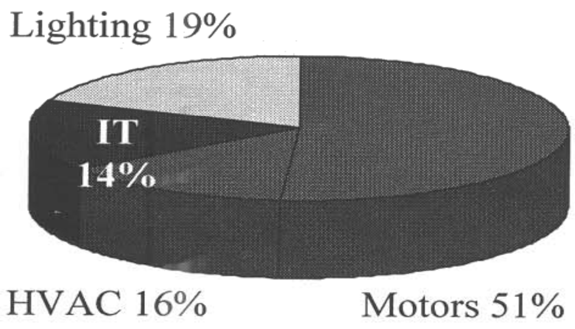


Figure 1-7 Percentage use of electricity in various sectors in the U.S.

1-3-1-1 Electric-Motor Driven Systems

Fig. 1-7 shows that electric motors, including their applications in heating, ventilating and air conditioning (HVAC), are responsible for consuming one-half to two-thirds of all the electricity generated. Traditionally, motor-driven systems run at a nearly constant speed and their output, for example, flow rate in a pump, is controlled by wasting a portion of the input energy across a throttling valve. This waste is eliminated by an adjustable-speed electric drive, as shown in Fig. 1-8 by efficiently controlling the motor speed, hence the pump speed, by means of power electronics [2].

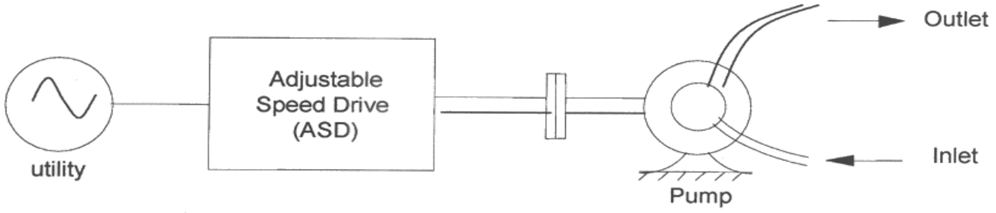


Figure 1-8 Role of adjustable speed drives in pump-driven systems.

One out of three new homes now uses electric heat pump, in which adjustable-speed drive can reduce energy consumption by as much as 30 percent [3] by eliminating on-off cycling of the compressor and running the heat pump at a speed that matches the thermal load of the building. The same is true for air conditioners.

A Department of Energy report [4] estimates that by operating all these motor-driven systems more efficiently in the United States could annually save electricity equivalent to the annual electricity usage by the entire state of New York!

1-3-1-2 Lighting

As shown in the pie chart in Fig. 1-7, approximately one-fifth of electricity produced is used for lighting. Fluorescent lights are more efficient than incandescent lights by a factor of three to four. The efficiency of fluorescent lights can be further improved by using high-frequency power electronic ballasts that supply 30 kHz to 40 kHz to the light bulb, as shown by the block diagram in Fig. 1-9, further increasing the efficiency by approximately 15 percent. Compared to incandescent light bulbs, high-frequency compact fluorescent lamps (CFLs) improve efficiency by a factor of four, last much longer (several thousand hours more), and their relative cost, although high at present, is dropping.

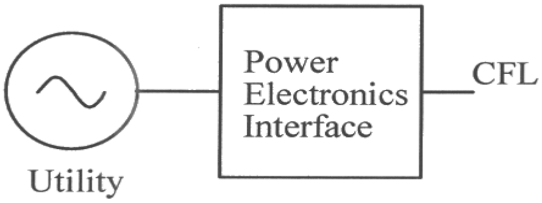


Figure 1-9 Power electronics interface required for CFL.

1-3-1-3 Transportation

Electric drives offer huge potential for energy conservation in transportation. While efforts to introduce commercially-viable Electric Vehicles (EVs) continue with progress in battery [5] and fuel cell technologies [6] being reported, hybrid electric vehicles (HEVs) are sure to make a huge impact [7]. According to the U.S. Environmental Protection Agency, the estimated gas mileage of the hybrid-electrical vehicle shown in Fig. 1-10 in combined city and highway driving is 48 miles per gallon [8]. This is in comparison to the gas mileage of 22.1 miles per gallon for an average passenger car in the U.S. in year 2001 [9]. Since automobiles are estimated to account for about 20% emission of all CO_2 [10] that is a greenhouse gas, doubling the gas mileage of automobiles would have an enormous impact on the environment.

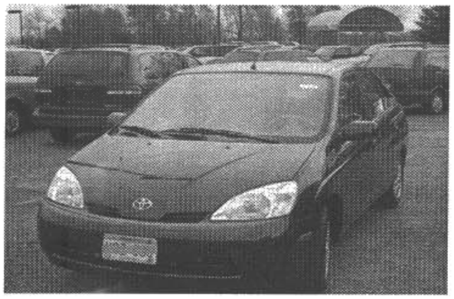
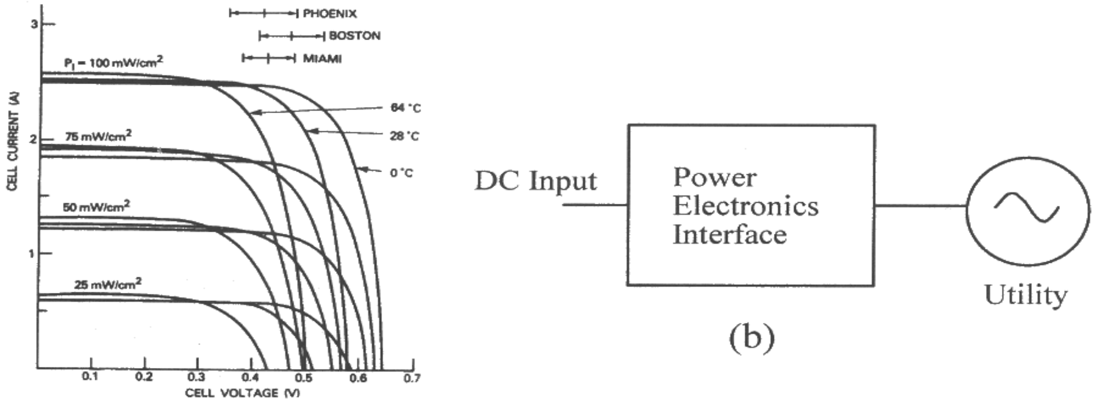


Figure 1-10 Hybrid electric vehicles with much higher gas mileage.

EVs and HEVs, of course, need power electronics in the form of adjustable-speed electric drives. Even in conventional automobiles, power electronic based load has grown to the extent that it is difficult to supply it from a 12/14-V battery system and there are serious proposals to raise it to 36/42-V level in order to keep the copper bus bars needed to carry currents a manageable size [11]. Add to this other transportation systems, such as light rail, fly-by-wire planes, all-electric ships and drive-by-wire automobiles, and transportation represents a major application area of power electronics.

1-3-2 Renewable Energy

Clean and renewable energy that is environmentally friendly can be derived from the sun and the wind. In photovoltaic systems, solar cells produce dc, with an *i-v* characteristic shown in Fig. 1-11a that requires a power electronics interface to transfer power into the utility system, as shown in Fig. 1-11b.



(a)

(b)

Figure 1-11 Photovoltaic Systems.

Wind is the fastest growing energy resource with enormous potential [12]. Fig. 1-12 shows the need of power electronics in wind-electric systems to interface variable-frequency ac to the line-frequency ac voltages of the utility grid.

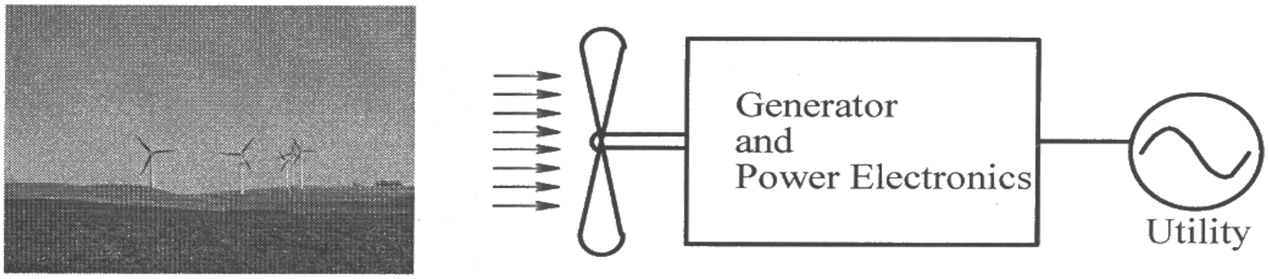


Figure 1-12 Wind-electric systems.

1-3-3 Utility Applications of Power Electronics

Applications of power electronics and electric drives in power systems are growing rapidly. In distributed generation, power electronics is needed to interface non-conventional energy sources such as wind, photovoltaic, and fuel cells to the utility grid. Use of power electronics allows control over the flow of power on transmission lines, an attribute that is especially significant in a deregulated utility environment. Also, the security and the efficiency aspects of power systems operation necessitate increased use of power electronics in utility applications.

Uninterruptible power supplies (UPS) are used for critical loads that must not be interrupted during power outages. The power electronics interface for UPS, shown in Fig. 1-13, has line-frequency voltages at both ends, although the number of phases may be different, and a means for energy storage is provided usually by batteries, which supply power to the load during the utility outage.

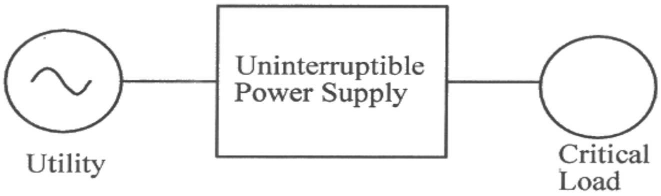


Figure 1-13 Uninterruptible power supply (UPS) system.

1-3-4 Strategic Space and Defense Applications

Power electronics is essential for space exploration and for interplanetary travel. Defense has always been an important application but it has become critical in the post-Sept 11th world. Power electronics will play a huge role in tanks, ships, and planes in which replacement of hydraulic drives by electric drives can offer significant cost, weight and reliability advantages.

1-4 NEED FOR HIGH EFFICIENCY AND HIGH POWER DENSITY

Power electronic systems must be energy efficient and reliable, have a high power density thus reducing their size and weight, and be low cost to make the overall system economically feasible. High energy efficiency is important for several reasons: it lowers operating costs by avoiding the cost of wasted energy, contributes less to global warming, and reduces the need for cooling (by heat sinks discussed later in this book) therefore increasing power density.

We can easily show the relationship in a power electronic system between the energy efficiency, η, and the power density. The energy efficiency is defined in Eq. 1-1 in terms of the output power P_o and the power loss P_{loss} within the system as

$$\eta = \frac{P_o}{P_o + P_{loss}} \tag{1-1}$$

Eq. 1-1 can be rewritten for the output power in terms of the efficiency and the power loss as

$$P_o = \frac{\eta}{1-\eta} P_{loss} \tag{1-2}$$

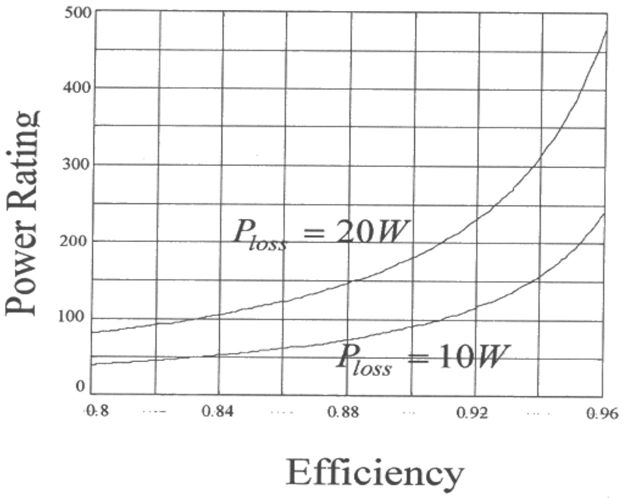


Figure 1-14 Power output capability as a function of efficiency.

In power electronics equipment, the cooling system is designed to transfer dissipated power, as heat, without allowing the internal temperatures to exceed certain limits. Therefore for a system designed to handle certain power loss, the plots in Fig. 1-14 based on Eq. 1-2 show that increasing the efficiency from 84% to 94% increases the power output capability (same as the power rating) of that equipment by a factor of three. This could mean an increase in the power density by approximately the same factor.

1-5 STRUCTURE OF POWER ELECTRONICS INTERFACE

By reviewing the role of power electronics in various applications discussed earlier, we can summarize that power electronics interface is needed to efficiently control the transfer of power between dc-dc, dc-ac, and ac-ac systems. In general, the power is supplied by the utility and hence, as depicted by the block diagram of Fig. 1-15, the line-frequency ac is at one end. At the other end, one of the following is synthesized: adjustable magnitude dc, sinusoidal ac of adjustable frequency and amplitude, or high frequency ac as in the case of compact fluorescent lamps (CFLs) and induction heating. Applications that do not require utility interconnection can be considered as the subset of the block diagram shown in Fig. 1-15.

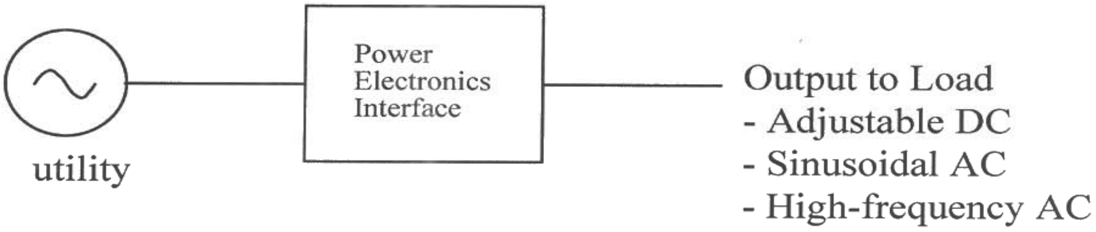


Figure 1-15 Block diagram of power electronic interface.

To provide the needed functionality to the interface in Fig. 1-15, the transistors and diodes, which can block voltage only of one polarity, have led to the structure shown in Fig. 1-16.

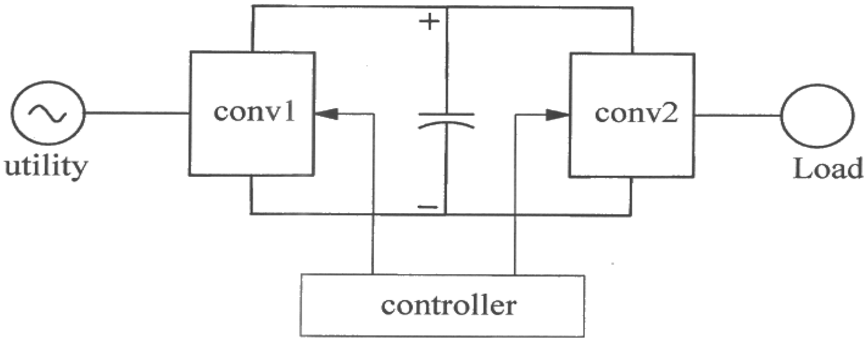


Figure 1-16 Voltage-link structure of power electronics interface.

This structure consists of two separate converters, one on the utility side and the other on the load side. The dc ports of these two converters are connected to each other with a parallel capacitor forming a dc-link, across which the voltage polarity does not reverse, thus allowing unipolar voltage handling transistors to be used within these converters. In certain applications, the power flow through these converters reverses, by currents reversing direction at the dc ports. The converter structure of Fig. 1-16 has the following benefits that explain their popularity:

- Decoupling of Two Converters: the voltage-port (dc-link) created by the capacitor in the middle decouples the operation of the utility-side and the load-side converters, thus allowing their design and operation to be optimized individually.
- Immunity from Momentary Power Interruptions: energy storage in the capacitor allows uninterrupted power flow to the load during momentary power-line disturbances. Continuing developments in increasing capacitor energy density further support this structure for the power electronics interface.

In the structure of Fig. 1-16, the capacitor in parallel with the two converters forms a dc voltage-link, hence this structure is called a *voltage-link* (or a *voltage-source*) structure. This structure is used in a very large power range, from a few tens of watts to several megawatts, even extending to hundreds of megawatts in utility applications. Therefore, we will mainly focus on this voltage-link structure in this book.

At extremely high power levels, usually in utility-related applications, which we will discuss in the last two chapters in this book, it may be advantageous to use a *current-link* (or a *current-source*) structure, where an inductor in series with the two converters acts as a current-link.

Lately in niche applications, a *matrix converter* structure is being reevaluated, where theoretically there is no energy storage element between the input and the output sides. Discussion of matrix converters is beyond the scope of this book on the first course on power electronics and drives.

1-6 THE SWITCH-MODE LOAD-SIDE CONVERTER

In the structure of Fig. 1-16, the role of the utility-side converter is to convert line-frequency utility voltages to an unregulated dc voltage. This can be done by a diode-rectifier circuit like that discussed in basic electronics courses, although power quality concerns may lead to a different structure discussed in Chapter 6. We will focus our attention on the load-side converter in the structure of Fig. 1-16, where a dc voltage is applied as an input on one end.

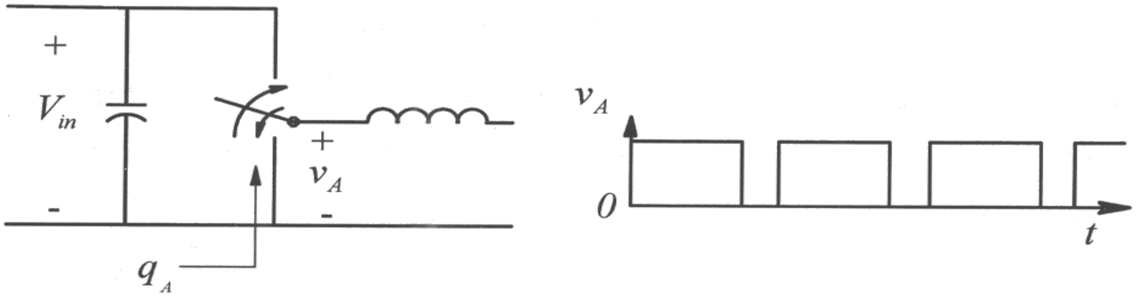
Applications dictate the functionality needed of the load-side converter. Based on the desired output of the converter, we can group this functionality as follows:

- Group 1 Adjustable dc or a low-frequency sinusoidal ac output in
  - dc and ac motor drives
  - uninterruptible power supplies
  - regulated dc power supplies without electrical isolation
- Group 2 High-frequency ac in
  - compact fluorescent lamps
  - induction heating
  - regulated dc power supplies where the dc output voltage needs to be electrically isolated from the input, and the load-side converter internally produces high-frequency ac, which is passed through a high-frequency transformer and then rectified into dc.

1-6-1 Switch-Mode Conversion: Switching Power-Pole as the Building Block

Achieving high energy-efficiency for applications belonging to either group mentioned above requires switch-mode conversion, where in contrast to linear power electronics, transistors (and diodes) are operated as switches, either on off.

This switch-mode conversion can be explained by its basic building block, a switching power-pole A, as shown in Fig. 1-17a. It effectively consists of a bi-positional switch, which forms a two-port: a voltage-port across a capacitor with a voltage V_{in} that cannot change instantaneously, and a current-port due the series inductor through which the current cannot change instantaneously. For now, we will assume the switch ideal with two positions: up or down, dictated by a switching signal q_A which takes on two values: 1 and 0, respectively. The practical aspects of implementing this bi-positional switch we will consider in the next chapter.



(a) (b)

Figure 1-17 Switching power-pole as the building block in converters.

The bi-positional switch "chops" the input dc voltage V_{in} into a train of high-frequency voltage pulses, shown by the v_A waveform in Fig. 1-17b, by switching up or down at a high repetition rate, called the switching frequency f_s. Controlling the pulse width within a switching cycle allows control over the average value of the pulsed output, and this pulse-width modulation forms the basis of synthesizing adjustable dc and low-frequency sinusoidal ac outputs, as described in the next section. High-frequency pulses are clearly needed in applications such as compact fluorescent lamps, induction heating, and internally in dc power supplies where electrical isolation is achieved by means of a high-frequency transformer. A switch-mode converter consists of one or more such switching power-poles.

1-6-2 Pulse-Width Modulation (PWM) of the Switching Power-Pole (constant f_s)

For the applications in Group 1, the objective of the switching power-pole redrawn in Fig. 1-18a is to synthesize the output voltage such that its *average* is of the desired value: dc or ac that varies sinusoidally at a low-frequency. Switching at a constant switching-frequency f_s produces a train of voltage pulses in Fig. 1-18b that repeat with a constant switching time-period T_s, equal to $1/f_s$.

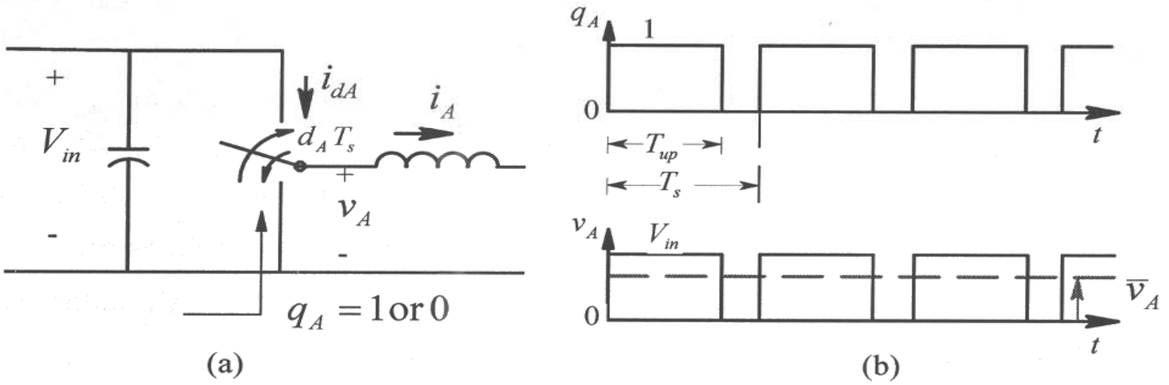


Figure 1-18 PWM of the switching power-pole.

Within each switching cycle with the time-period T_s $(=1/f_s)$ in Fig. 1-18b, the *average* value $\overline{v}_A$ of the waveform is controlled by the pulse width T_{up} during which the switch is in the up position, and v_A equals V_{in}:

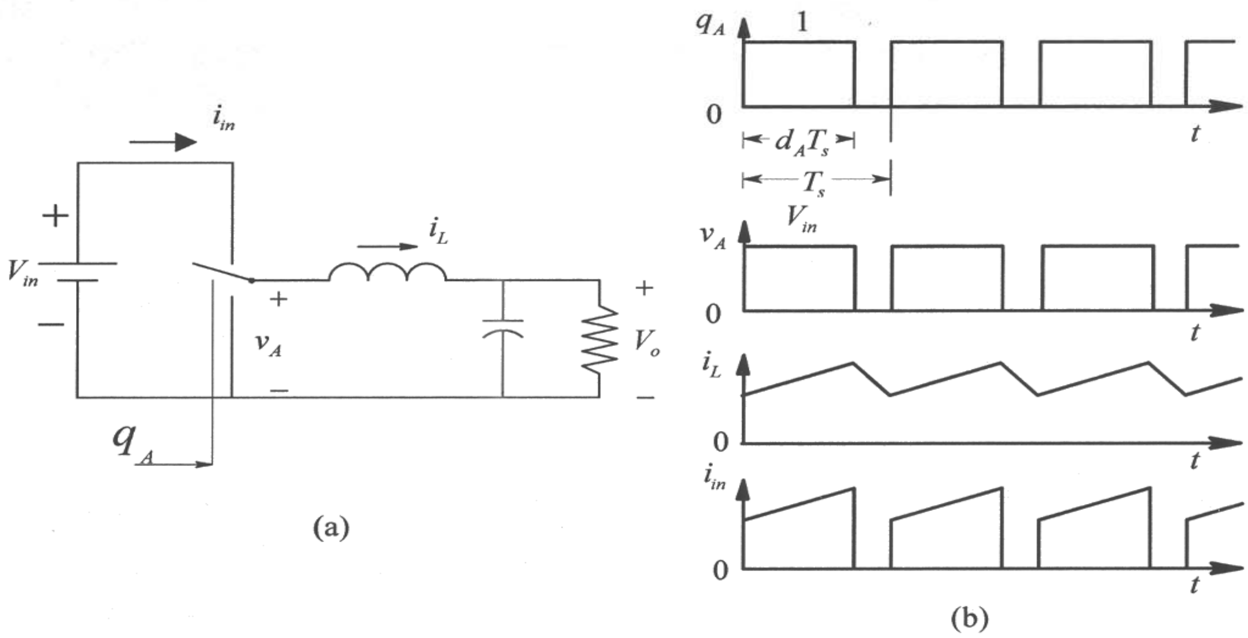
$$\overline{v}_A = \frac{T_{up}}{T_s} V_{in} = d_A V_{in} \qquad 0 \le d_A \le 1 \tag{1-3}$$

where $d_A (= T_{up}/T_s)$ is defined as the duty-ratio of the switching power-pole, and the average voltage is indicated by a "-" on top. The average voltage and the pole duty-ratio are expressed by lowercase letters since they may vary as functions of time. The control over the average value of the output voltage is achieved by adjusting or modulating the pulse width, which later on will be referred to as pulse-width-modulation (PWM). This switching power-pole and the control of its output by PWM set the stage for switch-mode conversion with high energy-efficiency.

We should note that $\overline{v}_A$ and d_A in the above discussion are discrete quantities and their values are to be calculated over each switching cycle. However in practical applications, the pulse-width T_{up} changes very slowly over many switching cycles, and hence we can consider them as analog quantities $\overline{v}_A(t)$ and $d_A(t)$ that are continuous functions of time. For simplicity, we may not show their time dependence explicitly.

1-6-3 Switching Power-Pole in a Buck DC-DC Converter: An Example

As an example, we will consider the switching power-pole in a *Buck* converter to step-down the input dc voltage V_{in}, as shown in Fig. 1-19a, where a capacitor is placed across the load to form a low-pass L-C filter to provide a smooth voltage to the load.



(a)

(b)

Figure 1-19 Switching power-pole in a Buck converter.

In steady state, the dc (average) input to this L-C filter has no attenuation, hence the average output voltage V_o equals the average, $\overline{v}_A$, of the applied input voltage. Based on Eq. 1-3, by controlling d_A, the output voltage can be controlled in a range from V_{in} down to 0:

$$V_o = \overline{v}_A = d_A V_{in} \qquad (0 \le V_o \le V_{in}) \tag{1-4}$$

In spite of the pulsating nature of the instantaneous output voltage $v_A(t)$, the series inductance at the current-port of the pole ensures that the current $i_L(t)$ remains relatively smooth, as shown in Fig. 1-19b.

1-6-3-1 Realizing the Bi-Positional Switch in a Buck Converter

As shown in Fig. 1-20a, the bi-positional switch in the power-pole can be realized by using a transistor and a diode. When the transistor is gated on (through a gate circuitry discussed in the next chapter by a switching signal $q_A = 1$), it carries the inductor current and the diode is reversed biased, as shown in Fig. 1-20b. When the transistor is switched off ($q_A = 0$), the inductor current "freewheels", as shown in Fig. 1-20c through the diode until the next switching cycle when the transistor is turned back on. The switching waveforms, shown earlier in Fig. 1-19b, are discussed in detail in Chapter 3.

In the switch-mode circuit of Fig. 1-19a, higher the switching frequency, that is the frequency of the pulses in the $v_A(t)$ waveform, smaller the values needed of the low-pass

L-C filter. On the other hand, higher switching frequency results in higher switching losses in the bi-positional switch, which is the subject of the next chapter. Therefore, an appropriate switching frequency must be selected, keeping these trade-offs in mind.

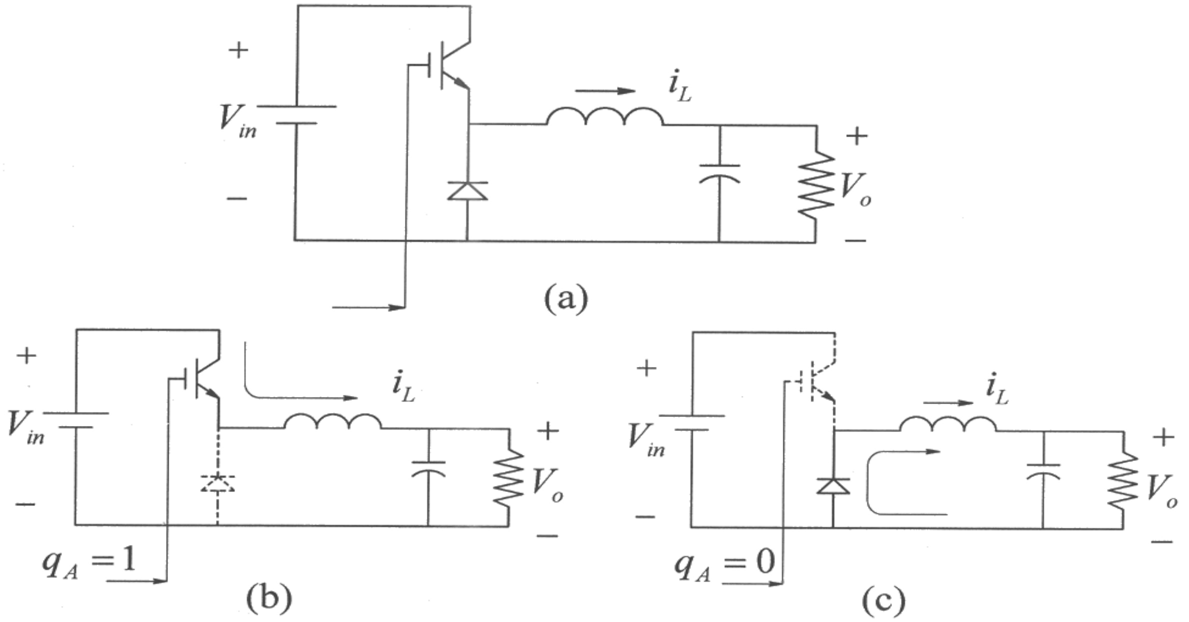


Figure 1-20 Transistor and diode forming a switching power-pole in a Buck converter.

1-7 RECENT AND POTENTIAL ADVANCEMENTS

Given the need in a plethora of applications, the rapid growth of this field is fueled by revolutionary advances in semiconductor fabrication technology. The power electronics interface of Fig. 1-1 consists of solid-state devices, which operate as switches, changing from on to off at a high frequency. There has been a steady improvement in the voltage and current handing capabilities of solid-state devices such as diodes and transistors, and their switching speeds (from on to off, and vice versa) have increased dramatically, with some devices switching in tens of *ns*. Devices that can handle voltages in kVs and currents in kAs are now available. These semiconductor switches are integrated in a single package with all the circuitry needed to make them switch, and to provide the necessary protection. Moreover, the costs of these devices are in a steady decline.

Power electronics has benefited from advances in the semiconductor fabrication technology in another important way. The availability of Application Specific Integrated Circuits (ASICs), Digital Signal Processor (DSPs), micro-controllers, and Field Programmable Gate Arrays (FPGA) at very low costs makes the controller function in the block diagram of Fig. 1-1 easy and inexpensive to implement, while greatly increasing functionality.

Significant areas for potential advancements in power electronic systems are in integrated and intelligent power modules, packaging, SiC-based solid-state devices, improved high energy density capacitors, and improved topologies and control.

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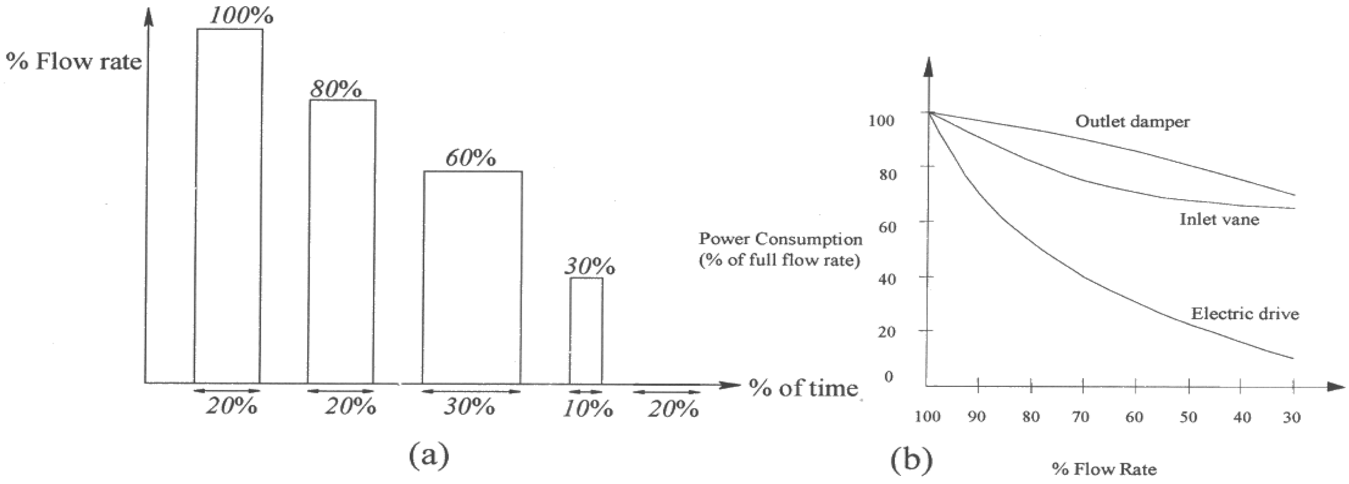
PROBLEMS

Applications and Energy Conservation

1-1 A U.S. Department of Energy report [4] estimates that over 122 billion kWh/year can be saved in the manufacturing sector in the United States by using mature and cost-effective conservation technologies. Calculate (a) how many 1000-MW generating plants are needed to operate constantly to supply this wasted energy, and (b) the annual savings in dollars if the cost of electricity is 0.10 $/kWh.

1-2 In a process, a blower is used with the flow-rate profile shown in Fig. P1-2a. Using the information in Fig P1-2b, estimate the percentage reduction in power consumption resulting from using an adjustable-speed drive rather than a system with (a) an outlet damper and (b) an inlet vane.



(a) (b)

Figure P1-2

1-3 In a system, if the system size is based on power dissipation capacity, calculate the improvement in the power density if the efficiency is increased from 85% to 95%.

1-4 According to [13], electricity generation in the U.S. in year 2000 was approximately 3.8×10^9 MW-hrs. Fig. 1-7 shows that 16% of that is used for heating, ventilating and air conditioning. Based on [3, 14], as much as 30% of the energy can be saved in such systems by using adjustable speed drives. On this basis, calculate the savings in energy per year and relate that to 1000-MW generating plants needed to operate constantly to supply this wasted energy.

1-5 According to [12], the total amount of electricity that could potentially be generated from wind in the United States has been estimated at 10.8×10^9 MW-hrs annually. If one-tenth of this potential is developed, estimate the number of 1-MW windmills that would be required, assuming the capacity factor of the windmills to be 25%.

1-6 In problem 1-5, if each 1-MW windmill has 20% of its output power flowing through the power electronics interface, estimate the total rating of these interfaces in kW.

1-7 As the pie chart of Fig. 1-7 shows, lighting in the U.S. consumes 19% of the generated electricity. Compact Fluorescent Lamps (CFLs) consume power onefourth of that consumed by the incandescent lamps for the same light output [15]. According to [13], electricity generation in the U.S. in year 2000 was approximately 3.8×10^9 MW-hrs. Based on this information, estimate the savings in MW-hrs annually, assuming that all lighting at present is by incandescent lamps, which are to be replaced by CFLs.

1-8 An electric-hybrid vehicle offers 52 miles per gallon in mixed (city and highway) driving conditions according to the U.S. Environmental Protection Agency. This is in comparison to the gas mileage of 22.1 miles per gallon for an average passenger car in the U.S. in year 2001 [9], with an average of 11,766 miles driven. Calculate the savings in terms of barrels of oil per automobile annually, if a conventional car is replaced by an electric-hybrid vehicle. In calculating this, assume that a barrel of oil that contains 42 gallons yields approximately 20 gallons of gasoline [16].

1-9 Based on the estimate in [17] of approximately 136 million automobiles in 1995, we can project that today there are 150 million cars in the U.S. Using the results of Problem 1-8, calculate the total annual reduction of carbon into the atmosphere, if the consumption of each gallon of gasoline releases approximately 5 pounds of carbon [16].

1-10 Relate the savings of barrels of oil annually, as calculated in Problem 1-9, to the imported oil, if the U.S. imports approximately 35,000 million barrels of crude oil per year [18].

1-11 Fuel-cell systems that also utilize the heat produced can achieve efficiencies approaching 80% [19], more than double of the gas-turbine based electrical generation. Assume that 25 million households produce an average of 5 kW. Calculate the percentage of electricity generated by these fuel-cell systems compared to the annual electricity generation in the U.S. of 3.8×10^9 MW-hrs [13].

1-12 Induction cooking based on power electronics is estimated to be 80% efficient compared to 55% for conventional electric cooking. If an average home consumes 2 kW-hrs daily using conventional electric cooking, and that 50 million households switch to induction cooking in the U.S., calculate the annual savings in electricity usage.

1-13 Assume the average energy density of sunlight to be 800 W/m^2 and the overall photovoltaic system efficiency to be 10%. Calculate the land area covered with photovoltaic cells needed to produce 1,000 MW, the size of a typical large central power plant.

1-14 In problem 1-13, the solar cells are distributed on top of roofs, each in area of 50 m^2. Calculate the number of homes needed to produce the same power.

PWM of the Switching Power-Pole

1-15 In a Buck converter, the input voltage $V_{in} = 12V$. The output voltage V_o is required to be $9V$. The switching frequency $f_s = 200kHz$. Assuming an ideal switching power-pole, calculate the pulse width T_{up} of the switching signal, and the duty-ratio d_A of the power pole.

1-16 In the Buck converter of Problem 1-15, assume the current through the inductor to be ripple-free with a value of $3A$ (the ripple in this current is discussed later in Chapter 3). Draw the waveforms of the voltage at the current-port and the input current at the voltage-port.

1-17 Using the input-output specifications given in Problems 1-15 and 1-16, calculate the maximum energy-efficiency expected of a linear regulator where the excess input voltage is dropped across a series element that behaves as a resistor.

Chapter 2

DESIGN OF SWITCHING POWER-POLES

In the previous chapter, we examined a switching power-pole as the building block of power electronic converters, consisting of an ideal bi-positional switch with an ideal transistor and an ideal diode, and pulse-width-modulated (PWM) to achieve regulation of the output. In this chapter, we will discuss the availability of various power semiconductor devices, their switching characteristics and various trade-offs in designing a switching power-pole. We will also briefly discuss a PWM-IC, which is used in regulating the average output of such switching power-poles.

2-1 POWER TRANSISTORS AND POWER DIODES [1]

The power-level diodes and transistors have evolved over decades from their signal-level counterparts to the extent that they can handle voltages and currents in kVs and kAs respectively, with fast switching times of the order of a few tens of ns to a few μs. Moreover, these devices can be connected in series and parallel to satisfy any voltage and current requirements.

Selection of power diodes and power transistors in a given application is based on the following characteristics:

1. Voltage Rating: the maximum instantaneous voltage that the device is required to block in its off-state, beyond which it "breaks down" and irreversible damage occurs.
2. Current Rating: the maximum current, expressed as instantaneous, average, and/or rms, that a device can carry in its on-state, beyond which excessive heating within the device destroys it.
3. Switching Speeds: the speeds with which a device can make a transition from its on-state to off-state, or vice versa. Small switching times associated with fast-switching devices result in low switching losses, or considering it differently, fast-switching devices can be operated at high switching frequencies with acceptable switching power losses.
4. On-State Voltage: the voltage drop across a device during its on-state while conducting a current. The smaller this voltage, the smaller will be the on-state power loss.

2-2 SELECTION OF POWER TRANSISTORS [2-5]

Transistors are controllable switches, which are available in several forms for switch-mode power electronics applications:

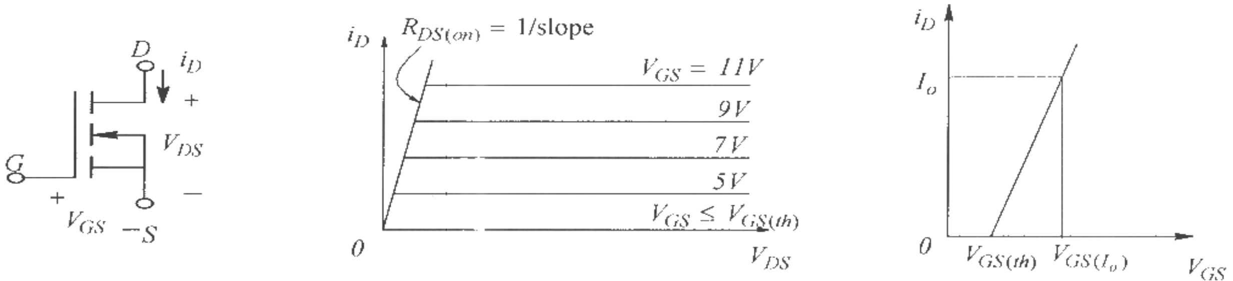
- MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors)
- IGBTs (Insulated-Gate Bipolar Transistors)
- IGCTs (Integrated-Gate-Controlled Thyristors)
- GTOs (Gate-Turn-Off thyristors)
- Niche devices for power electronics applications, such as BJTs (Bipolar-Junction Transistors), SITs (Static Induction Transistors), MCTs (MOS-Controlled Thyristors), and so on.

In switch-mode converters, there are two types of transistors which are primarily used: MOSFETs are typically used below a few hundred volts at switching frequencies in excess of 100 kHz, whereas IGBTs dominate very large voltage, current and power ranges extending to MW levels, provided the switching frequencies are below a few tens of kHz. IGCTs and GTOs are used in utility applications of power electronics at power levels beyond a few MWs. The following subsections provide a brief overview of MOSFET and IGBT characteristics and capabilities.

2-2-1 MOSFETs

In applications at voltages below 200 volts and switching frequencies in excess of 100 kHz, MOSFETs are clearly the device of choice because of their low on-state losses in low voltage ratings, their fast switching speeds, and a high impedance gate which requires a small voltage and charge to facilitate on/off transition. The circuit symbol of an n-channel MOSFET is shown in Fig. 2-1a. It consists of three terminals: drain (D), source (S), and gate (G). The forward current in a MOSFET flows from the drain to the source terminal. MOSFETs can block only the forward polarity voltage, that is, a positive v_{DS}. They cannot block a negative-polarity voltage due to an intrinsic anti-parallel diode, which can be used effectively in most switch-mode converter designs. MOSFET i-v characteristics for various gate voltage values are shown in Fig. 2-1b.

For gate voltages below a threshold value $v_{GS(th)}$, typically in a range of 2 to 4 V, a MOSFET is completely off, as shown by the i-v characteristics in Fig. 2-1b, and approximates an open switch. Beyond $v_{GS(th)}$, the drain current i_D through the MOSFET depends on the applied gate voltage v_{GS}, as shown by the transfer characteristic shown in Fig. 2-1c, which is valid almost for any value of the voltage v_{DS} across the MOSFET (note the horizontal nature of i-v characteristics in Fig. 2-1b). To carry $i_D (= I_o)$ would require a gate voltage of a value, at least equal to $v_{GS(I_o)}$, as shown in Fig. 2-1c. Typically, a higher gate voltage, approximately 10 V, is maintained in order to keep the MOSFET in its on-state and carrying $i_D(=I_o)$.



(a) (b) (c)

Figure 2-1 MOSFET: (a) symbol, (b) *i-v* characteristics, (c) transfer characteristic.

In its on-state, a MOSFET approximates a very small resistor $R_{DS(on)}$, and the drain current that flows through it depends on the external circuit in which it is connected. The on-state resistance, inverse of the slope of i - v characteristics as shown in Fig. 2-1b, is a strong function of the blocking voltage rating V_{DSS} of the device:

$$R_{DS(on)}\ \alpha\ V_{DSS}^{2.5 to 2.7} \tag{2-1}$$

The relationship in Eq. 2-1 explains why MOSFETs in low-voltage applications, at less than 200 V, are an excellent choice. The on-state resistance goes up with the junction temperature within the device and proper heatsinking must be provided to keep the temperature below the design limit.

2-2-2 IGBTs

IGBTs combine the ease of control, as in MOSFETs, with low on-state losses even at fairly high voltage ratings. Their switching speeds are sufficiently fast for switching frequencies up to 30 kHz. Therefore, they are used for converters in a vast voltage and power range - from a fractional kW to several MWs where switching frequencies required are below a few tens of kHz.

The circuit symbol for an IGBT is shown in Fig. 2-2a and the i - v characteristics are shown in Fig. 2-2b. Similar to MOSFETs, IGBTs have a high impedance gate, which requires only a small amount of energy to switch the device. IGBTs have a small on-state voltage, even in devices with large blocking-voltage rating, for example, V_{on} is approximately 2 V in 1200-V devices.

IGBTs can be designed to block negative voltages, but most commercially available devices, by design to improve other properties, cannot block any appreciable reverse-polarity voltage. IGBTs have turn-on and turn-off times on the order of a microsecond and are available as modules in ratings as large as 3.3 kV and 1200 A. Voltage ratings of up to 5 kV are projected.

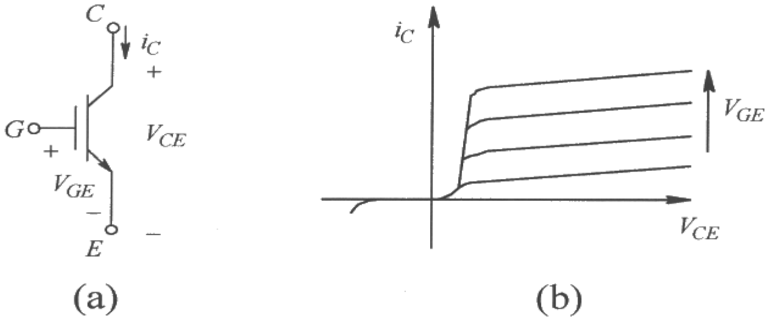


Figure 2-2 IGBT: (a) symbol, (b) *i*-*v* characteristics.

2-2-3 Power-Integrated Modules and Intelligent-Power Modules [2-4]

Power electronic converters, for example for three-phase ac drives, require six power transistors. Power-integrated modules (PIMs) combine several transistors and diodes in a single package. Intelligent-power modules (IPMs) include power transistors with the gate-drive circuitry. The input to this gate-drive circuitry is a signal that comes from a microprocessor or an analog integrated circuit, and the output drives the MOSFET gate. IPMs also include fault protection and diagnostics, thereby immensely simplifying the power electronics converter design.

2-2-4 Costs of MOSFETs and IGBTs

As these devices evolve, their relative costs continue to decline. The costs of single devices are approximately 0.25 $/A for 600-V devices and 0.50 $/A for 1200-V devices. Power modules for the 3 kV class of devices cost approximately 1 $/A.

2-3 SELECTION OF POWER DIODES

The circuit symbol of a diode is shown in Fig. 2-3a and its i - v characteristic in Fig. 2-3b shows that a diode is an uncontrolled device that blocks reverse polarity voltage. Power diodes are available in large ranges of reverse voltage blocking and forward current carrying capabilities. Similar to transistors, power diodes are available in several forms as follows, and their selection must be based on their application:

- Line-frequency diodes
- Fast-recovery diodes
- Schottky diodes
- SiC-based Schottky diodes

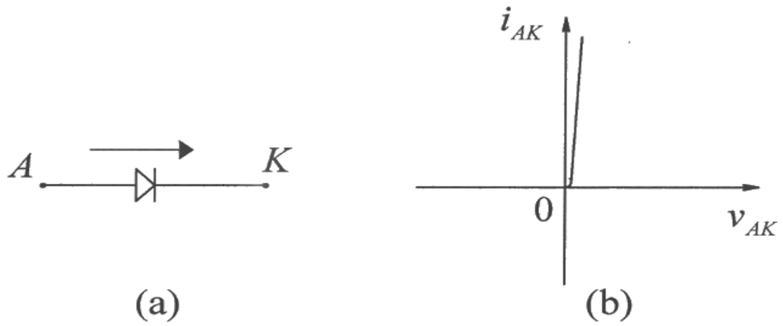


Figure 2-3 Diode: (a) symbol, (b) *i*-*v* characteristic.

Rectification of line-frequency ac to dc can be accomplished by slower switching *p*-*n* junction power (line-frequency) diodes, which have relatively a slightly lower on-state voltage drop, and are available in voltage ratings of up to 9 kV and current ratings of up to 5 kA. The on-state voltage drop across these diodes is usually on the order of 1 to 3 V, depending on the voltage blocking capability.

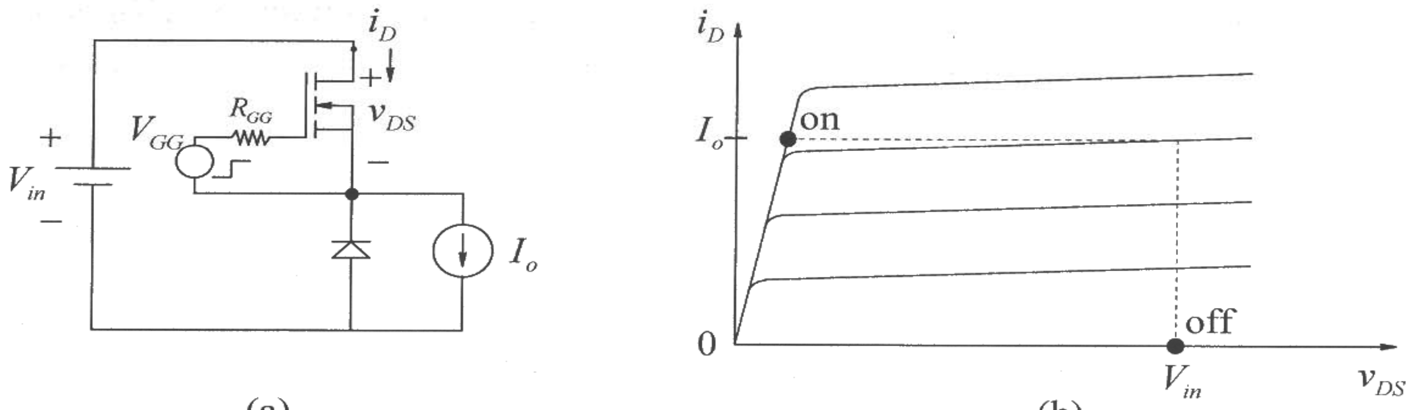
Switch-mode converters operating at high switching frequencies, from several tens of kHz to several hundred kHz, require fast-switching diodes. In such applications, fast-recovery diodes, also formed by *p*-*n* junction as the line-frequency diodes, must be selected to minimize switching losses associated with the diodes.

In applications with very low output voltages, the forward voltage drop of approximately a volt or so across the conventional p-n junction diodes becomes unacceptably high. In such applications, another type of device called the Schottky diode is used with a voltage drop in the range of 0.3 to 0.5 V. Being majority-carrier devices, Schottky diodes switch extremely fast and keep switching losses to a minimum.

All devices, transistors and diodes, discussed above are silicon based. Lately, silicon-carbide (SiC) based Schottky diodes in voltage ratings of up to 600 V have become available [6]. In spite of their large on-state voltage drop (1.7 V, for example), their capability to switch with a minimum of switching losses makes them attractive in converters with voltages in excess of a few hundred volts.

2-4 SWITCHING CHARACTERISTICS AND POWER LOSSES IN POWER-POLES

In switch-mode converters, it is important to understand switching characteristics of the switching power-pole. As discussed in the previous chapter, the power-pole in a Buck converter shown in Fig. 2-4a is implemented using a transistor and a diode, where the current through the current port is assumed a constant dc, I_o, for discussing switching characteristics. We will assume the transistor to be a MOSFET, although a similar discussion applies if an IGBT is selected.



(a) (b)

Figure 2-4 MOSFET in a switching power-pole.

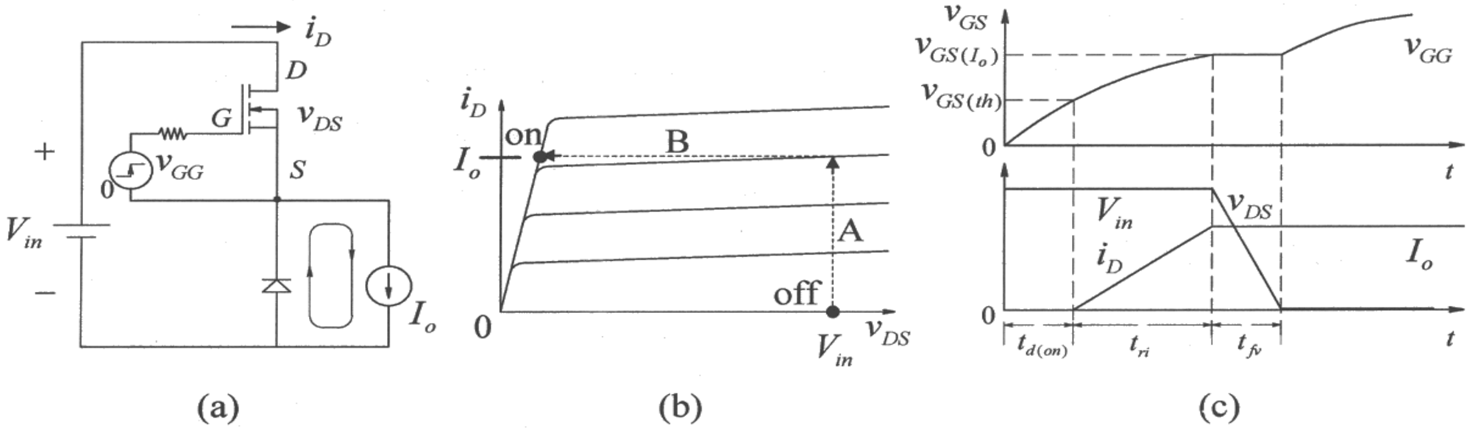
For the n-channel MOSFET (p-channel MOSFETs have poor characteristics and are seldom used in power applications), the typical i_D versus v_{DS} characteristics are shown in Fig. 2-4b for various gate voltages. The off-state and the on-state operating points are labeled on these characteristics.

Switching characteristics of MOSFETs, hence of the switching power-pole in Fig. 2-4a are dictated by a combination of factors: the speed of charging and discharging of junction capacitances within the MOSFET, i_D versus v_{DS} characteristics, the circuit of Fig. 2-4a in which the MOSFET is connected and its gate-drive circuitry. We should note that the MOSFET junction capacitances are highly nonlinear functions of drain-source voltage and go up dramatically by several orders of magnitude at lower voltages. In Fig. 2-4a, the gate-drive voltage for the MOSFET is represented as a voltage source, which changes from 0 to V_{GG}, approximately 10 V, and vice versa, and charges or discharges the gate through a resistance R_{gate} that is the sum of an external resistance R_{GG} and the internal gate resistance.

Only a simplified explanation of the turn-on and turn-off characteristics, assuming an ideal diode, is presented here. The switching details including the diode reverse recovery are discussed in the Appendix to this chapter.

2-4-1 Turn-on Characteristic

Prior to turn-on, Fig. 2-5a shows the circuit in which the MOSFET is off and blocks the input dc voltage V_{in}; I_o "freewheels" through the diode. By applying a positive voltage to the gate, the turn-on characteristic describes how the MOSFET goes from the off-point to the on-point in Fig. 2-5b. To turn the MOSFET on, the gate-drive voltage goes up from 0 to V_{GG}, and it takes the gate-drive a finite amount of time, called the turn-on delay-time $t_{d(on)}$, to charge the gate-source capacitance through the gate-circuit resistance R_{gate} to the threshold value of $V_{GS(th)}$. During this turn-on delay time, the MOSFET remains off and I_o continues to freewheel through the diode, as shown in Fig. 2-5a.



(a) (b) (c)

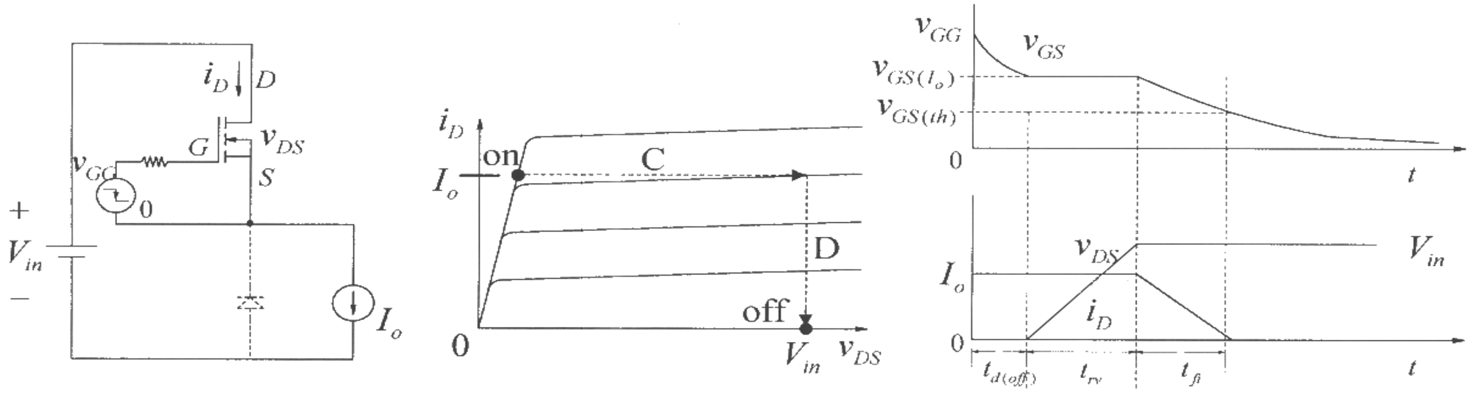
Figure 2-5 MOSFET turn-on.

For the MOSFET to turn on, first the current i_D through it rises. As long as the diode is conducting a positive net current $(I_o - i_D)$, the voltage across it is zero and the MOSFET must block the entire input voltage V_{in}. Therefore, during the current rise-time t_{ri}, the MOSFET voltage and the current are along the trajectory A in the i-v characteristics of Fig. 2-5b, and are plotted in Fig. 2-5c. Once the MOSFET current reaches I_o, the diode becomes reverse biased, and the MOSFET voltage falls. During the voltage fall-time t_{fv}, as depicted by the trajectory B in Fig. 2-5b and the plots in Fig. 2-5c, the gate-to-source voltage remains at $V_{GS(I_o)}$. Once the turn-on transition is complete, the gate charges to the gate-drive voltage V_{GG}, as shown in Fig. 2-5c.

2-4-2 Turn-off Characteristic

The turn-off sequence is opposite to the turn-on process. Prior to turn-off, the MOSFET is conducting I_o and the diode is reversed biased as shown in Fig. 2-6a. The MOSFET i-v characteristics are re-plotted in Fig 2-6b. The turn-off characteristic describes how the MOSFET goes from the on-point to the off-point in Fig. 2-6b. To turn the MOSFET off, the gate-drive voltage goes down from V_{GG} to 0. It takes the gate-drive a finite amount of time, called the turn-off delay-time $t_{d(off)}$, to discharge the gate-source capacitance through the gate-circuit resistance R_{gate}, from a voltage of V_{GG} to $V_{GS(I_o)}$. During this turn-off delay time, the MOSFET remains on.

For the MOSFET to turn off, the output current must be able to "freewheel" through the diode. This requires the diode to become forward biased, and thus the voltage across the MOSFET must rise as shown by the trajectory C in Fig. 2-6b, while the current through it remains I_o. During this voltage rise-time t_{rv}, the voltage and current are plotted in Fig. 2-6c, while the gate-to-source voltage remains at $V_{GS(I_o)}$. Once the voltage across the MOSFET reaches V_{in}, the diode becomes forward biased, and the MOSFET current falls. During the current fall-time t_{fi}, depicted by the trajectory D in Fig. 2-6b and the plots in Fig. 2-6c, the gate-to-source voltage declines to $V_{GS(th)}$. Once the turn-off transition is complete, the gate discharges to 0.



(a) (b) (c)

Figure 2-6 MOSFET turn-off.

2-4-3 Calculating Power Losses Within the MOSFET (assuming an ideal diode)

Power losses in the gate-drive circuitry are negligibly small except at very high switching frequencies. The primary source of power losses is across the drain and the source, which can be divided into two categories: the conduction loss, and the switching losses. Both of these are discussed in the following sections.

2-4-3-1 Conduction Loss

In the on-state, the MOSFET conducts a drain current for an interval T_{on} during every switching time-period T_s, with the switch duty-ratio $d = T_{on} / T_s$. Assuming this current a constant I_o during $d T_s$, the average power loss in the on-state resistance $R_{DS(on)}$ of the MOSFET is:

$$P_{cond} = d \, R_{DS(on)} I_o^2 \tag{2-2}$$

As pointed out earlier, $R_{DS(on)}$ varies significantly with the junction temperature and data sheets often provide its value at the junction temperature equal to 25^oC. However, it will be more realistic to use twice this resistance value that corresponds to the junction temperature equal to 120^0C, for example. Eq. 2-2 can be refined to account for the effect of ripple in the drain current on the conduction loss. The conduction loss is highest at the maximum load on the converter when the drain current would also be at its maximum.

2-4-3-2 Switching Losses

At high switching frequencies, switching power losses can be even higher than the conduction loss. The switching waveforms for the MOSFET voltage v_{DS} and the current i_D, corresponding to the turn-on and the turn-off trajectories in Figs. 2-5 and 2-6, assumed linear with time, are re-plotted in Fig. 2-7. During each transition from on to off, and vice versa, the transistor has simultaneously high voltage and current, as seen from the switching waveforms in Fig. 2-7. The instantaneous power loss $p_{sw}(t)$ in the transistor is the product of v_{DS} and i_D, as plotted. The average value of the switching losses from the plots in Fig. 2-7 is

$$P_{sw} = \frac{1}{2} V_{in} I_o (t_{c,on} + t_{c,off}) f_s \qquad (2\text{-}3)$$

where $t_{c,on}$ and $t_{c,off}$ are defined in Fig. 2-7 as the sum of the rise and the fall times associated with the MOSFET voltage and current:

$$t_{c,on} = t_{ri} + t_{fv} \qquad (2\text{-}4)$$

$$t_{c,off} = t_{rv} + t_{fi} \qquad (2\text{-}5)$$

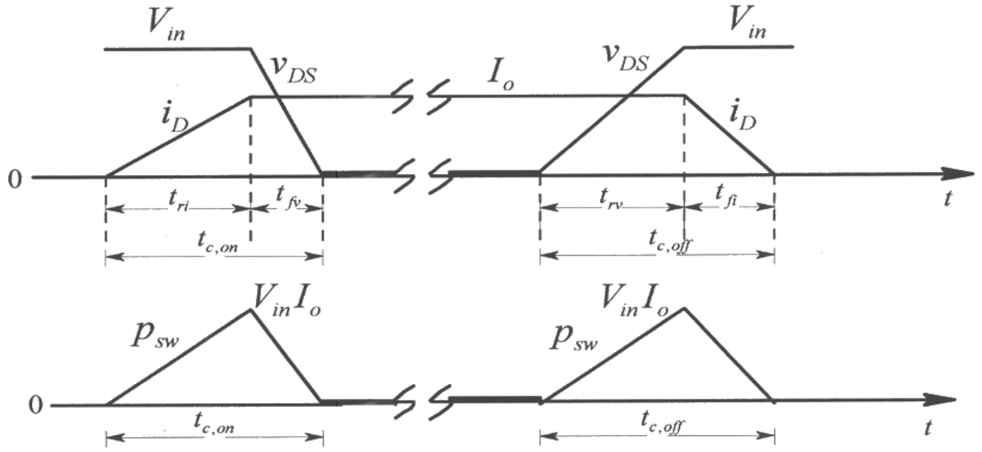


Figure 2-7 MOSFET switching losses.

▲ **Example 2-1** Assuming an ideal diode, calculate losses in a MOSFET for the following operating conditions in the power-pole of Fig. 2-4a: $V_{in} = 40V$, $I_o = 5A$, $d = 0.4$, and $f_s = 300kHz$. Assume that the switching times $t_{c,on} = t_{c,off} = 25ns$. The on-state resistance $R_{DS(on)} = 0.3\Omega$. Also calculate the percentage efficiency of the converter based just on the losses in the MOSFET.

Solution From Eq. 2-2, the average conduction power loss is $P_{cond} = d\,R_{DS(on)} I_o^2 = 3W$. From Eq. 2-3, using Eqs. 2-4 and 2-5, the average switching power loss is $P_{sw} = 0.5 \times V_{in} I_o (t_{c,on} + t_{c,off}) f_s = 1.5W$. Therefore, the total power loss $P_{loss} = 4.5W$. The output voltage of the converter is $V_o = d\,V_{in} = 16V$. The output power $P_o = V_o I_o = 80W$. From Eq. 1-1 of Chapter 1, the converter efficiency based on the MOSFET power losses is $\eta = 94.67\%$.

2-4-4 Gate Driver Integrated Circuits (ICs) with Built-in Fault Protection [2]

Application-Specific ICs (ASICs) for controlling the gate voltages of MOSFETs and IGBTs greatly simplify converter design by including various protection features, for example, the over-current protection that turns off the transistor under fault conditions. This functionality, as discussed earlier, is integrated into Intelligent Power Modules along with the power semiconductor devices.

The IC to drive the MOSFET gate is shown in Fig. 2-8 in a block diagram form. To drive the high-side MOSFET in the power-pole, the input signal v_c from the controller is referenced to the logic level ground, V_{CC} is the logic supply voltage, and V_{ext} to drive the gate is supplied by an isolated power supply referenced to the MOSFET source S.

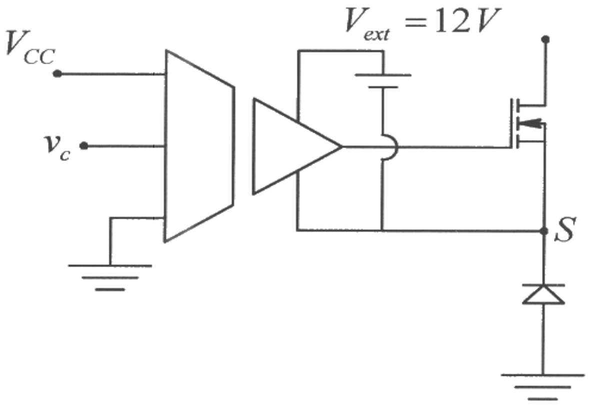


Figure 2-8 Gate-driver IC functional diagram.

One of the ICs for this purpose is IR2127, which can source 200 mA for gate charging and sink 420 mA for gate discharging, with typical turn-on and turn-off times of 200 ns and 150 ns, respectively. This IC, although it has relatively large switching times, may be a good choice due to its easy-to-use fault protection capability, in which the transistor current, measured via the voltage drop across a small resistance in series with the transistor, disables the gate-drive voltage under over-current conditions.

2-5 JUSTIFYING SWITCHES AND DIODES AS IDEAL

Product reliability and high energy-efficiency are two very important criteria. In designing converters, it is essential that in the selection of semiconductor devices, we consider their voltage and current ratings with proper safety margins for reliability purposes. Achieving high energy-efficiency from converters requires that in selecting power devices, we consider their on-state voltage drops and their switching characteristics. We also need to calculate the heat that needs to be removed for proper thermal design.

Typically, the converter energy efficiency of approximately 90 percent or higher is realized. This implies that semiconductor devices have a very small loss associated with them. Therefore, in analyzing various converter topologies and comparing them against each other, we can assume transistors and diodes ideal. Their non-idealities, although essential to consider in the actual selection and the subsequent design process, represent a second-order phenomena, that will be ignored in analyzing various converter topologies. We will use a generic symbol shown earlier for transistors, regardless of their type, and ignore the need for a specific gate-drive circuitry.

2-6 DESIGN CONSIDERATIONS

In designing any converter, the overall objectives are to optimize their cost, size, weight, energy efficiency, and the reliability. With these goals in mind, we will briefly discuss some important considerations as the criteria for selecting the topology and the components in a given application.

2-6-1 Switching Frequency f_s

As discussed in the Buck converter example of the previous chapter, a switching power-pole results in a waveform pulsating at a high switching frequency at the current-port. The high frequency components in the pulsating waveform need to be filtered. It is intuitively obvious that the benefits of increasing the switching frequencies lie in reducing the filter component values, L and C, hence their physical sizes in a converter. (This is true up to a certain value, for example, up to a few hundred kHz, beyond which, for example, magnetic losses in inductors and the internal inductance within capacitors reverse the trend.) Hence, higher switching frequencies allow a higher control bandwidth, as we will see in Chapter 4.

The negative consequences of increasing the switching frequency are in increasing the switching losses in the transistor and the diode, as discussed earlier. Higher switching frequencies also dictate a faster switching of the transistor by appropriately designed gate-drive circuitry, generating greater problems of electromagnetic interference due to higher di/dt and dv/dt that introduce switching noise in the control loop. We can minimize these problems, at least in dc-dc converters, by adopting a soft-switching topology discussed in Chapter 10.

2-6-2 Selection of Transistors and Diodes

Earlier we discussed the voltage and the switching frequency ranges for selecting between MOSFETs and IGBTs. Similarly, the diode types should be chosen appropriately. The voltage rating of these devices is based on the peak voltage $\hat{V}$ in the circuit (including voltage spikes due to parasitic effects during switching). The current ratings should consider the peak current $\hat{I}$ that the devices can handle and which dictates the switching power loss, the rms current I_{rms} for MOSFETs which behave as a resistor with $R_{DS(on)}$ in their on-state, and the average current I_{avg} for IGBTs and diodes, which can be approximated to have a constant on-state voltage drop. Safety margins, which depend on the application, dictate that the device ratings be greater than the worst-case stresses by a certain factor.

2-6-3 Magnetic components

As discussed earlier, the filter inductance value depends on the switching frequency. Inductor design is discussed later in Chapter 9, which shows that the physical size of a filter inductor, to a first approximation, depends on a quantity called the area-product (A_p) given by the equation below:

$$A_p = L\hat{I}I_{rms} \tag{2-6}$$

Increasing L in many topologies reduces the peak and the rms values (also reducing the transistor and the diode current stresses) but has the negative consequence of increasing the overall inductor size and possibly reducing the control bandwidth.

2-6-4 Capacitor Selection [7]

Capacitors have switching losses designated by an equivalent series resistance, ESR, as shown in Fig. 2-9. They also have an internal inductance, represented as an equivalent series inductance, ESL. The resonance frequency, the frequency beyond which ESL begins to dominate C, depends on the capacitor type. Electrolytic capacitors offer high capacitance per unit volume but have low resonance frequency. On the other hand, capacitors such as metal-polypropylene have relatively high resonance frequency.

Therefore, in switch-mode dc power supplies, an electrolytic capacitor with high C may often be paralleled with a metal-polyester capacitor to form the output filter capacitor.

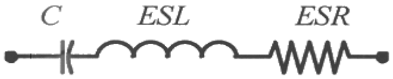


Figure 2-9 Capacitor ESR and ESL.

2-6-5 Thermal Design [8, 9]

Power dissipated in the semiconductor and the magnetic devices must be removed to limit temperature rise within the device. The reliability of converters and their life expectancy depend on the operating temperatures, which should be well below their maximum allowed values. On the other hand, letting them operate at a high temperature decreases the cost and the size of the heat sinks required. There are several cooling techniques but for general-purpose applications, converters are often designed for cooling by normal air convection, without the use of forced air or liquid.

Semiconductor devices come in a variety of packages, which differ in cost, ruggedness, thermal conduction, and the radiation hardness if the application demands it. Fig. 2-10a shows a semiconductor device affixed to a heat sink through an isolation pad that is thermally conducting but provides electrical isolation between the device case and the heat sink.

An analogy can be drawn with an electrical circuit of Fig. 2-10b where the power dissipation within the device is represented as a dc current source, thermal resistances offered by various paths are represented as series resistances, and the temperatures at various points as voltages. The data sheets specify various thermal resistance values. The heat transfer mechanism is primarily conduction from the semiconductor device to its case and through the isolation pad. The resulting thermal resistances can be represented by $R_{\theta jc}$ and $R_{\theta cs}$, respectively. From the heat sink to the ambient, the heat transfer mechanisms are primarily convection and radiation, and the thermal resistance can be represented by $R_{\theta sa}$. Based on the electrical analogy, the junction temperature can be calculated as follows for the dissipated power P_{diss}:

$$T_j = T_a + (R_{\theta jc} + R_{\theta cs} + R_{\theta sa})P_{diss} \tag{2-7}$$

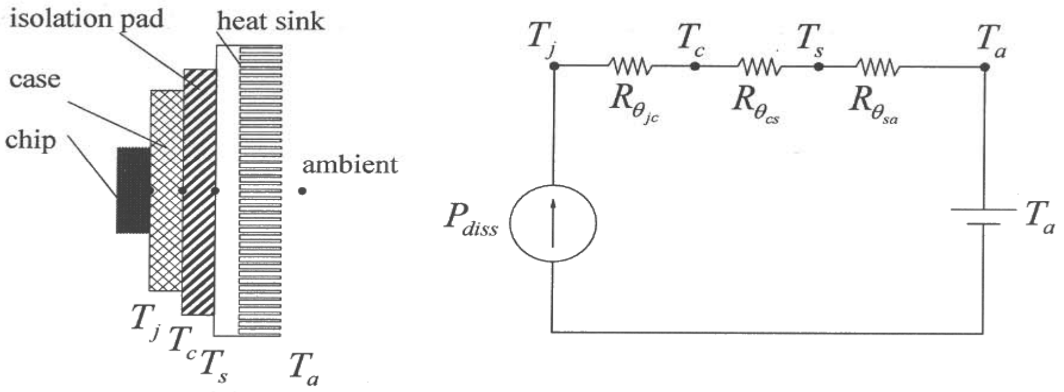


Figure 2-10 Thermal design: (a) semiconductor on a heat sink, (b) electrical analog.

2-6-6 Design Tradeoffs

As a function of switching frequency, Fig. 2-11 qualitatively shows the plot of physical sizes for the magnetic components and the capacitors, and the heat sink. Based on the present state-of-the-art, optimum values of switching frequencies to minimize the overall size in dc-dc converters using MOSFETs range from 200 kHz to 300 kHz with a slight upward trend.

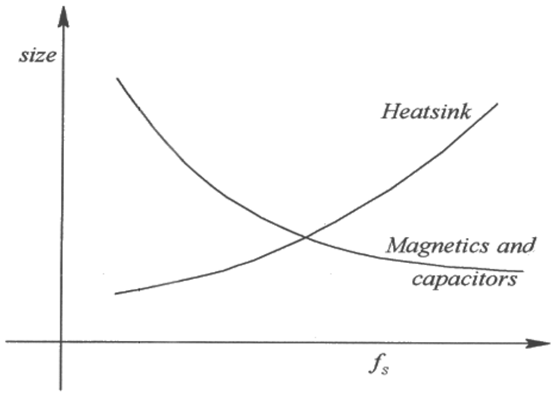


Figure 2-11 Size of magnetic components and heat sink as a function of frequency.

2-7 THE PWM IC [10]

In the pulse-width-modulation of the power-pole in a dc-dc converter, a high speed PWM IC such as the UC3824 from Unitrode/Texas Instruments may be used. Functionally within this PWM-IC, the control voltage $v_c(t)$ generated by the controller is compared with a ramp signal v_r of amplitude $\hat{V}_r$, at a constant switching frequency f_s, as shown in Fig. 2-12. The output switching signal represents the transistor switching function $q(t)$, which equals 1 if $v_c(t) \geq v_r$; otherwise 0. The transistor duty-ratio based on Fig. 2-12 is given as

$$d(t) = \frac{v_c(t)}{\hat{V}_r} \tag{2-8}$$

Thus, the control voltage $v_c(t)$ can provide regulation of the average output voltage of the switching power-pole, as discussed further in Chapters 3 and 4.

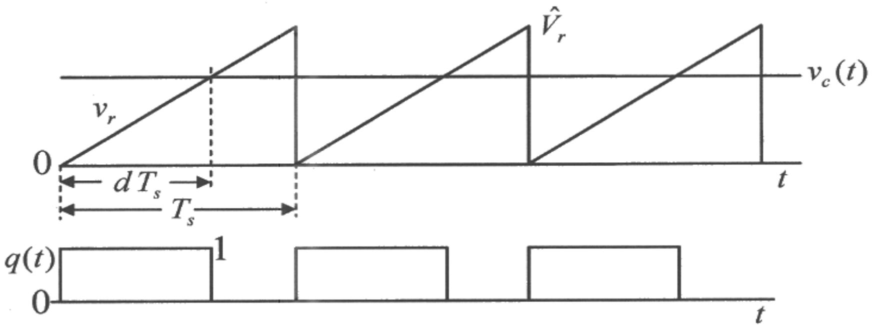


Figure 2-12 PWM IC waveforms.

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PROBLEMS

MOSFET in a Power-Pole of Fig 2-4a

A MOSFET is used in a switching power-pole shown in Fig. 2-4a. Assume the diode ideal. The operating conditions are as follows: $V_{in} = 40V$, $I_o = 5A$, the switching frequency $f_s = 200kHz$, and the duty-ratio $d = 0.3$. Under the operating conditions, the MOSFET has the following switching times: $t_{d(on)} = 100ns$, $t_{ri} = 30ns$, $t_{fv} = 20ns$,

$t_{d(off)} = 50ns$, $t_{rv} = 25ns$, $t_{fi} = 15ns$. The on-state resistance of the MOSFET is $R_{DS(on)} = 20m\Omega$. Assume V_{GG} as a step voltage between 0 V and 12 V.

2-1 Draw and label the turn-on and turn-off characteristics of the MOSFET and sketch the MOSFET gate-source voltage v_{GS} waveform.

2-2 Plot the turn-on and the turn-off switching power losses in the MOSFET. Calculate the average switching power loss in the MOSFET, and the percentage reduction in the converter energy efficiency due to this switching power loss.

2-3 Calculate the average conduction loss in the MOSFET.

2-4 In stead of an ideal diode, consider that the diode is actual and has a forward voltage drop $V_{FM} = 0.8V$. Calculate the average forward power loss in the diode.

2-5 In the diode reverse recovery characteristic shown in Fig. 2A-1, $t_a = 10ns$, $t_{rr} = 25ns$, and $I_{RRM} = 2A$. Calculate the average switching power in the diode.

2-6 In the gate-drive circuitry of the MOSFET, assume that the external power supply V_{ext} in Fig. 2-8 has a voltage of 12 V. Each time, to turn the MOSFET *on* under the conditions given requires a charge $Q_g = 45nC$. Calculate the average gate-drive power loss.

2-7 In this problem, we will calculate new values of the turn-on and the turn-off delay times of the MOSFET, based on the gate driver IC IR2127, as described in section 2-4-4. This IC is supplied with a voltage $V_{ext} = 12V$ with respect to the MOSFET *Source*. Assume this voltage to equal V_{GG}.

(a) For the turn-on, assume that this driver IC is a voltage source of V_{GG} with an internal resistance of 60Ω in series. Calculate the turn-on delay time $t_{d(on)}$, assuming that the MOSFET threshold voltage $V_{GS(th)} = 3V$. Assume the MOSFET capacitance to be 1190 pF for this calculation.

(b) For turning-off of the MOSFET, assume that this driver IC shorts the MOSFET gate to its source through an internal resistance of 30Ω. Calculate the turn-off delay time $t_{d(off)}$, assuming that the MOSFET voltage $V_{GS(I_o)} = 4.5V$. Assume the MOSFET capacitance to be 1900 pF for this calculation.

2-8 In the Buck converter in which this switching power-pole is used, the output filter capacitor consists of a parallel combination of an electrolytic capacitor and a metalized-polyester capacitor. The electrolytic capacitor has the following measured values: $C = 697\,\mu F$, $\mathrm{ESR} = 0.037\,\Omega$, and $\mathrm{ESL} = 16\,nH$. The metalized-polyester capacitor has the following measured values: $C = 10\,\mu F$, $\mathrm{ESR} = 0.04\,\Omega$, and $\mathrm{ESL} = 34\,nH$. Using any computer program, plot the impedance magnitude of each capacitor, and of their parallel combination, on the same log-log plot, as a function of frequency (from 1 kHz to 1 MHz). At $f_s = 200\,kHz$, what are the relative impedance magnitudes of these two capacitors?

2-9 The MOSFET losses are the sum of those computed in Problems 2-2 and 2-3. The junction temperature must not exceed $100^0 C$, and the ambient temperature is given as $40^0 C$. From the MOSFET datasheet, $R_{\theta jc} = 1.2^0 C/W$. The thermal pad has $R_{\theta cs} = 1.8^0 C/W$. Calculate the maximum value of $R_{\theta sa}$ that the heat sink can have.

APPENDIX 2A DIODE REVERSE RECOVERY AND POWER LOSSES

In this appendix, the diode reverse characteristic is described and the associated power losses are calculated. The increase in the MOSFET turn-on switching loss due to the diode reverse recovery current is discussed in the accompany CD.

2A-1 Average Forward Loss in Diodes

The current flow through a diode results in a forward voltage drop V_{FM} across the diode. The average forward power loss $P_{diode,F}$ in the diode in the circuit of Fig. 2-4a can be calculated as

$$P_{diode,F} = (1-d)\cdot V_{FM} I_o \tag{2A-1}$$

where d is the MOSFET duty-ratio in the power-pole, and hence the diode conducts for ($1-d$) portion of each switching time-period.

2A-2 Diode Reverse Recovery Characteristic

Forward current in power diodes, unlike in Schottky diodes that are majority-carrier devices, is due to the flow of electrons as well as holes. This current results in an accumulation of electrons in the p-region and of holes in the n-region. The presence of these charges allows a flow of current in the negative direction that sweeps away these excess charges, and the negative current quickly comes to zero, as shown in the plot of Fig. 2A-1. The peak reverse recovery current I_{RRM} and the reverse recovery charge Q_{rr} shown in Fig. 2A-1 depend on the initial forward current I_o and the rate di/dt at which this current decreases.

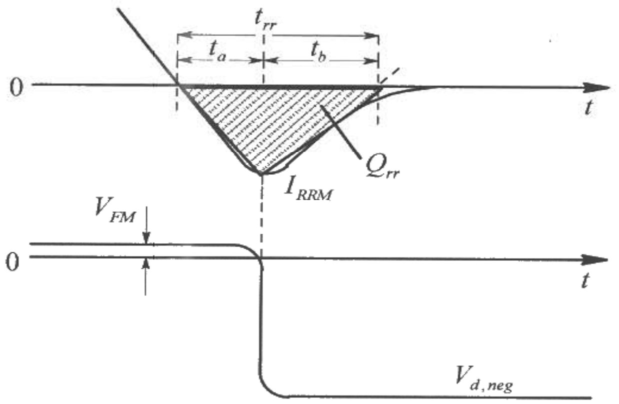


Figure 2A-1 Diode reverse recovery characteristic.

2A-3 Diode Switching Losses

The reverse recovery current results in switching losses within the diode when a negative current is flowing beyond the interval t_a in Fig. 2A-1, while the diode is blocking a negative voltage $V_{d,neg}$. This switching power loss in the diode can be estimated from the plots of Fig. 2A-1 as

$$P_{diode,sw} = (\frac{1}{2} I_{RRM} t_b) \cdot V_{d,neg} \cdot f_s \tag{2A-2}$$

where f_s is the switching frequency. In switch-mode power electronics, increase in switching losses due to the diode reverse recovery can be significant, and diodes with ultra-fast reverse recovery characteristics are needed to avoid these from becoming excessive.

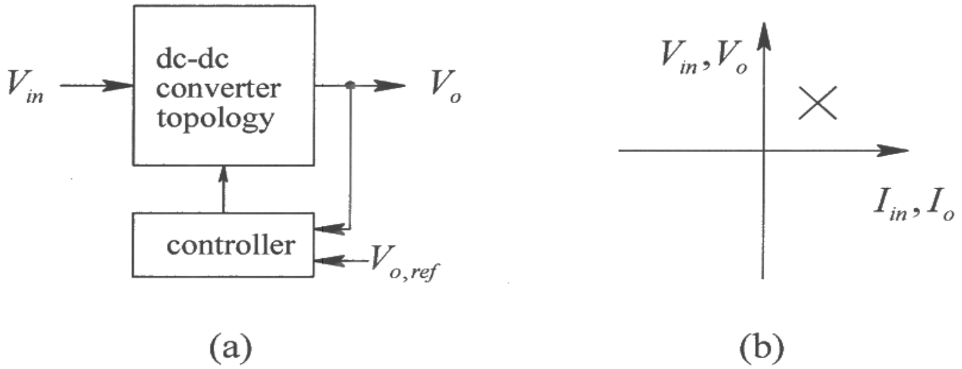
The reverse recovery current of the diode also increases the turn-on losses in the associated MOSFET of the power-pole, as discussed in the accompanying CD.

Chapter 3

SWITCH-MODE DC-DC CONVERTERS: SWITCHING ANALYSIS, TOPOLOGY SELECTION AND DESIGN

3-1 DC-DC CONVERTERS [1]

In Chapter 1, we discussed the need for Buck, Boost, and Buck-Boost dc-dc converters, shown by the block diagram of Fig. 3-1a, and how the pulse-width modulation process regulates the output voltage. The design of the feedback controller is the subject of the next chapter. The power flow through these converters is in only one direction, thus their voltages and currents remain unipolar and unidirectional, as shown in Fig. 3-1b. Based on these converters, several transformer-isolated dc-dc converter topologies, which are used in all types of electronics equipment, are discussed in Chapter 8.



(a) (b)

Figure 3-1 Regulated switch-mode dc power supplies.

3-2 SWITCHING POWER-POLE IN DC STEADY STATE

All the converters that we will discuss consist of a switching power-pole that was introduced in Chapter 1, and is redrawn in Fig. 3-2a. In these converter circuits in dc steady state, the input voltage and the output load are assumed constant. The switching power-pole operates with a transistor switching function $q(t)$, whose waveform repeats, unchanged from one cycle to the next, and the corresponding switch duty-ratio remains constant at its dc steady state value D. Therefore, all waveforms associated with the power-pole repeat with the switching time-period T_s in the dc steady state, where the basic principles described below are extremely useful for analysis purposes.

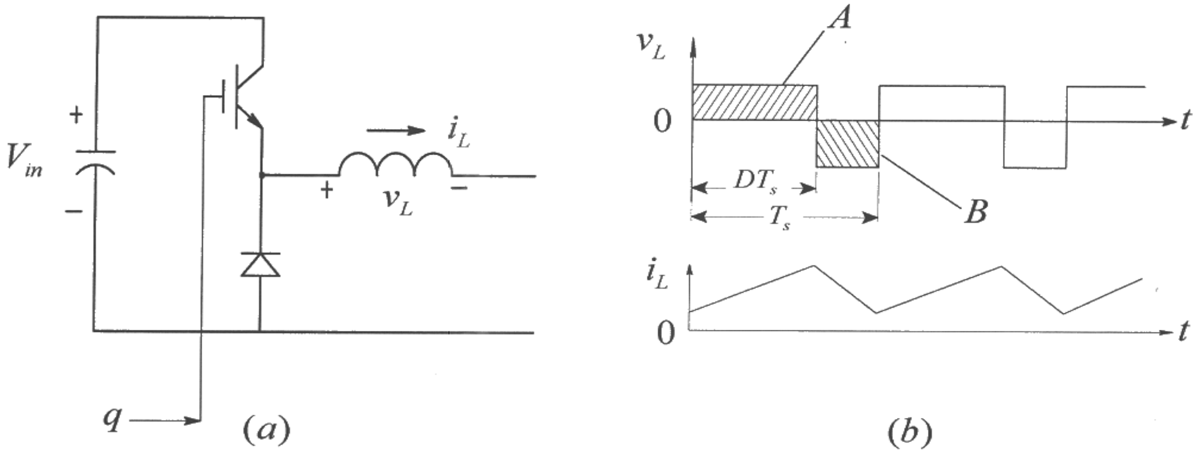


Figure 3-2 Switching power-pole as the building block of dc-dc converters.

First, let us consider the voltage and current of the inductor associated with the power-pole. The inductor current depends on the pulsating voltage waveform shown in Fig. 3-2b. The inductor voltage and current are related by the conventional differential equation, which can be expressed in the integral form as follows:

$$v_L = L\frac{di_L}{dt} \qquad \Rightarrow \qquad i_L(t) = \frac{1}{L}\int_{\tau} v_L \cdot d\tau \tag{3-1}$$

where τ, representing time, is a variable of integration. For simplicity, we will consider the first time-period starting with $t = 0$ in Fig. 3-2b. Using the integral form in Eq. 3-1, the inductor current at a time t can be expressed in terms of its initial value $i_L(0)$ as:

$$i_L(t) = i_L(0) + \frac{1}{L}\int_0^t v_L \cdot d\tau \tag{3-2}$$

In the dc steady state, the waveforms of all circuit variables must repeat with the switching frequency time-period T_s, resulting in the following conclusions from Eq. 3-2:

1. The inductor current waveforms repeats with T_s, and therefore in Eq. 3-2

$$i_L(T_s) = i_L(0) \tag{3-3}$$

2. Integrating over one switching time-period T_s in Eq. 3-2 and using Eq. 3-3 show that the inductor voltage integral over T_s is zero. This leads to the conclusion that the average inductor voltage, averaged over T_s, is zero:

$$\frac{1}{L}\int_0^{T_s} v_L \cdot d\tau = 0 \qquad \Rightarrow \qquad V_L = \frac{1}{T_s}(\underbrace{\int_0^{DT_s} v_L \cdot d\tau}_{\text{area } A} + \underbrace{\int_{DT_s}^{T_s} v_L \cdot d\tau}_{\text{area } B}) = 0 \tag{3-4}$$

In Fig. 3-2a, the area A in volt-s, that causes the current to rise, equals in magnitude the negative area B that causes the current to decline to its initial value.

The above analysis applies to any inductor in a switch-mode converter circuit operating in a dc steady state. By analogy, a similar analysis applies to any capacitor in a switch-mode converter circuit, operating in the dc steady state, as follows: the capacitor voltage and current are related by the conventional differential equation, which can be expressed in the integral form as follows:

$$i_C = C\frac{dv_C}{dt} \quad \Rightarrow \quad v_C(t) = \frac{1}{C}\int_{\tau} i_C \cdot d\tau \tag{3-5}$$

where τ, representing time, is a variable of integration. Using the integral form of Eq. 3-5, the capacitor voltage at a time t can be expressed in terms of its initial value $v_C(0)$ as:

$$v_C(t) = v_C(0) + \frac{1}{C}\int_0^t i_C \cdot d\tau \tag{3-6}$$

In the dc steady state, the waveforms of all circuit variables must repeat with the switching frequency time-period T_s, resulting in the following conclusions from Eq. 3-6:

1. The capacitor voltage waveform repeats with T_s, and therefore in Eq. 3-6

$$v_C(T_s) = v_C(0) \tag{3-7}$$

2. Integrating over one switching time-period T_s in Eq. 3-6 and using Eq. 3-7 show that the capacitor current integral over T_s is zero, which leads to the conclusion that the average capacitor current, averaged over T_s, is zero:

$$\frac{1}{C}\int_0^{T_s} i_C \cdot d\tau = 0 \quad \Rightarrow \quad I_C = \frac{1}{T_s}\int_0^{T_s} i_C \cdot d\tau = 0 \tag{3-8}$$

In addition to the above two conclusions, it is important to recognize that in dc steady state, just like for instantaneous quantities, the Kirchhoff's voltage and current laws apply to average quantities as well. In the dc steady state, average voltages sum to zero in a circuit loop, and average currents sum to zero at a node:

$$\sum_k V_k = 0 \tag{3-9}$$

$$\sum_k I_k = 0 \tag{3-10}$$

3-3 SIMPLIFYING ASSUMPTIONS

To gain a clear understanding in the dc steady state, we will first make certain simplifying assumptions by ignoring the second-order effects listed below, and later on include them for accuracy:

1. Transistors, diodes and other passive components are all ideal unless explicitly stated. For example, we will ignore the inductor equivalent series resistance.
2. The input is a pure dc voltage V_{in}.
3. Design specifications require the ripple in the output voltage to be very small. Therefore, we will initially assume that the output voltage is purely dc without any ripple, that is $v_o(t) \simeq V_o$, and later calculate the ripple in it.
4. The current at the current-port of the power-pole through the series inductor flows continuously, resulting in a continuous conduction mode, CCM (the discontinuous conduction mode, DCM, is analyzed later on).

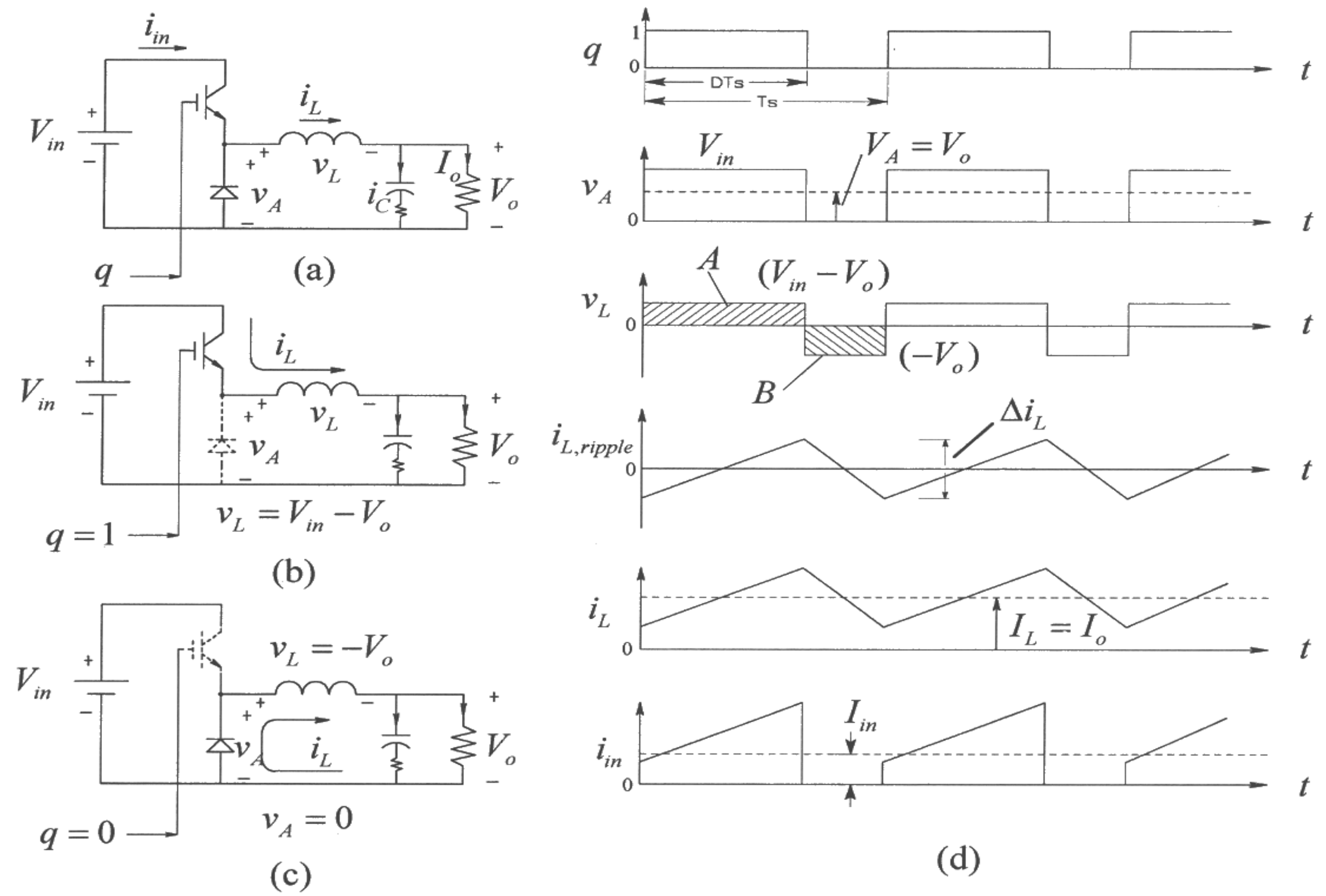
It is, of course possible to analyze a switching circuit in detail, without making the above simplifying assumptions as we will do in computer simulations. However, the two-step approach followed here, where the analysis is first carried out by neglecting the second-order effects and adding them later on, provides a deeper insight into converter operation and the design tradeoffs.

3-4 COMMON OPERATING PRINCIPLES

In all three converters that we will analyze, the inductor associated with the switching power-pole acts as an energy transfer means from the input to the output. Turning on the transistor of the power-pole increases the inductor energy by a certain amount, drawn from the input source, which is transferred to the output stage during the off-interval of the transistor. In addition to this inductive energy-transfer means, depending on the converter, there may be additional energy transfer directly from the input to the output, as discussed in the following sections.

3-5 BUCK CONVERTER SWITCHING ANALYSIS IN DC STEADY STATE

A Buck converter is shown in Fig. 3-3a, with the transistor and the diode making up the bi-positional switch of the power-pole. The equivalent series resistance (ESR) of the capacitor will be ignored. Turning on the transistor increases the inductor current in the sub-circuit of Fig. 3-3b. When the transistor is turned off, the inductor current "freewheels" through the diode, as shown in Fig. 3-3c.



i_{in}
V_{in}
i_L
v_L
v_A
i_C
I_o
V_o
q
(a)
V_{in}
i_L
v_L
v_A
V_o
$v_L = V_{in} - V_o$
$q = 1$
(b)
$v_L = -V_o$
V_{in}
v_A
i_L
V_o
$q = 0$
$v_A = 0$
(c)
q
1
0
DTs
Ts
t
v_A
V_{in}
$V_A = V_o$
0
t
v_L
A
$(V_{in} - V_o)$
0
t
B
$(-V_o)$
Δi_L
$i_{L,ripple}$
0
t
i_L
0
$I_L = I_o$
t
I_{in}
i_{in}
0
t
(d)

Figure 3-3 Buck dc-dc converter.

For a given transistor switching function waveform $q(t)$ shown in Fig. 3-3d with a switch duty-ratio D in steady state, the waveform of the voltage v_A at the current-port follows $q(t)$ as shown. In Fig. 3-3d, integrating v_A over T_s, the average voltage V_A equals DV_{in}. Recognizing that the average inductor voltage is zero (Eq. 3-4) and the average voltages in the output loop sum to zero (Eq. 3-9),

$$V_o = V_A = DV_{in} \tag{3-11}$$

The inductor voltage v_L pulsates between two values, $(V_{in} - V_o)$ and $(-V_o)$ as plotted in Fig. 3-3d. Since the average inductor voltage is zero, the volt-second areas during two sub-intervals are equal in magnitude and opposite in sign. In dc steady state, the inductor current can be expressed as the sum of its average and the ripple component:

$$i_L(t) = I_L + i_{L,ripple}(t) \tag{3-12}$$

where the average current depends on the output load, and the ripple component is dictated by the waveform of the inductor voltage v_L in Fig. 3-3d. As shown in Fig. 3-3d, the ripple component consists of linear segments, rising when v_L is positive and falling when v_L is negative. The peak-peak ripple can be calculated as follows, using either area A or B:

$$\Delta i_L = \frac{1}{L}\underbrace{(V_{in} - V_o)DT_s}_{\text{Area A}} = \frac{1}{L}\underbrace{V_o(1-D)T_s}_{\text{Area B}} \tag{3-13}$$

This ripple component is plotted in Fig. 3-3d. Since the average capacitor current is zero in dc steady state, the average inductor current equals the output load current by the Kirchhoff's current law applied at the output node:

$$I_L = I_o = \frac{V_o}{R} \tag{3-14}$$

The inductor current waveform is shown in Fig. 3-3d by superposing the average and the ripple components.

Next, we will calculate the ripple current through the output capacitor. In practice, the filter capacitor is large to achieve the output voltage nearly dc $(v_o(t) \simeq V_o)$. Therefore, to the ripple-frequency current, the path through the capacitor offers much smaller impedance than through the load resistance, hence justifying the assumption that the ripple component of the inductor current flows entirely through the capacitor. That is, in Fig. 3-3a

$$i_C(t) \simeq i_{L,ripple}(t) \tag{3-15}$$

In practice, the voltage drops across the capacitor ESR and the ESL dominate over the voltage drop $\frac{1}{C}\int i_C dt$ across C. The capacitor current i_C, equal to $i_{L,ripple}$ in Fig. 3-3d, can be used to calculate the ripple in the output voltage.

The input current i_{in} pulsates, equal to i_L when the transistor is on, otherwise zero, as plotted in Fig. 3-3d. An input L-C filter is often needed to prevent the pulsating current from being drawn from the input dc source. The average value of the input current in Fig. 3-3d is

$$I_{in} = DI_L = DI_o \qquad (\text{using Eq. 3-14}) \tag{3-16}$$

Using Eqs. 3-11 and 3-16, we can confirm that the input power equals the output power, as it should, in this idealized converter:

$$V_{in}I_{in} = V_o I_o \tag{3-17}$$

Eq. 3-11 shows that the voltage conversion ratio of Buck converters in the continuous conduction mode (CCM) depends on D, but is independent of the output load. If the output load decreases (that is, if the load resistance increases) to the extent that the inductor current becomes discontinuous, then the input-output relationship in CCM is no longer valid, and, if the duty-ratio D were to be held constant, the output voltage in the discontinuous-conduction mode would rise above that given by Eq. 3-11. The discontinuous conduction mode will be considered fully in section 3-15 and in the Appendix to this chapter.

3-6 BOOST CONVERTER SWITCHING ANALYSIS IN DC STEADY STATE

A Boost converter is shown in Fig. 3-4a. Compared to a Buck converter, it has two major differences:

1. Power flow is from a lower voltage dc input to the higher load voltage, in the opposite direction through the switching power-pole. Hence, the current direction through the series inductor of the power pole is chosen as shown, opposite to that in a Buck converter, and this current remains positive in the continuous conduction mode.
2. In the switching power-pole, the bi-positional switch is realized using a transistor and a diode that are placed as shown in Fig. 3-4a. Across the output, a filter capacitor C is placed, which forms the voltage port and minimizes the output ripple voltage.

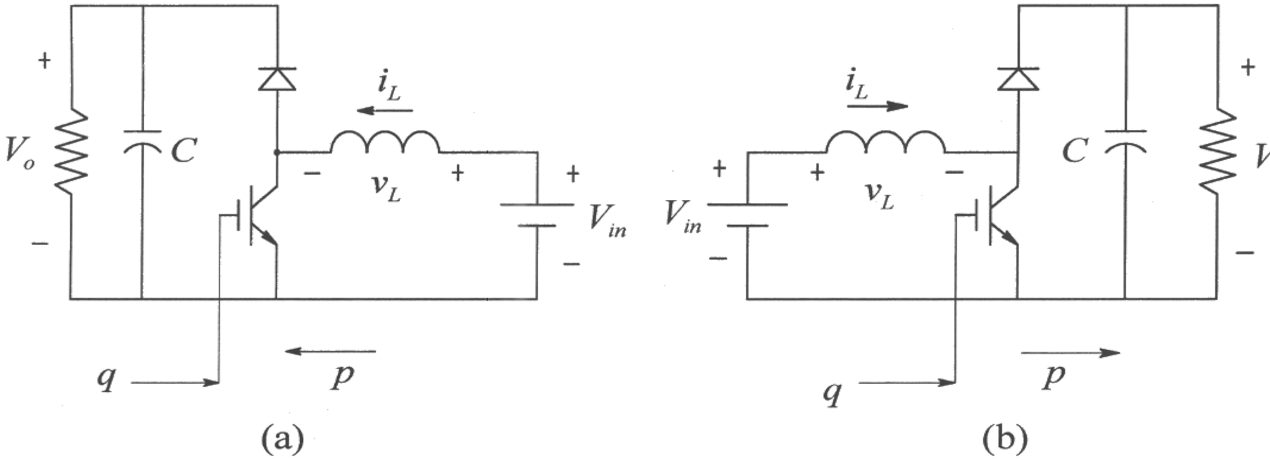
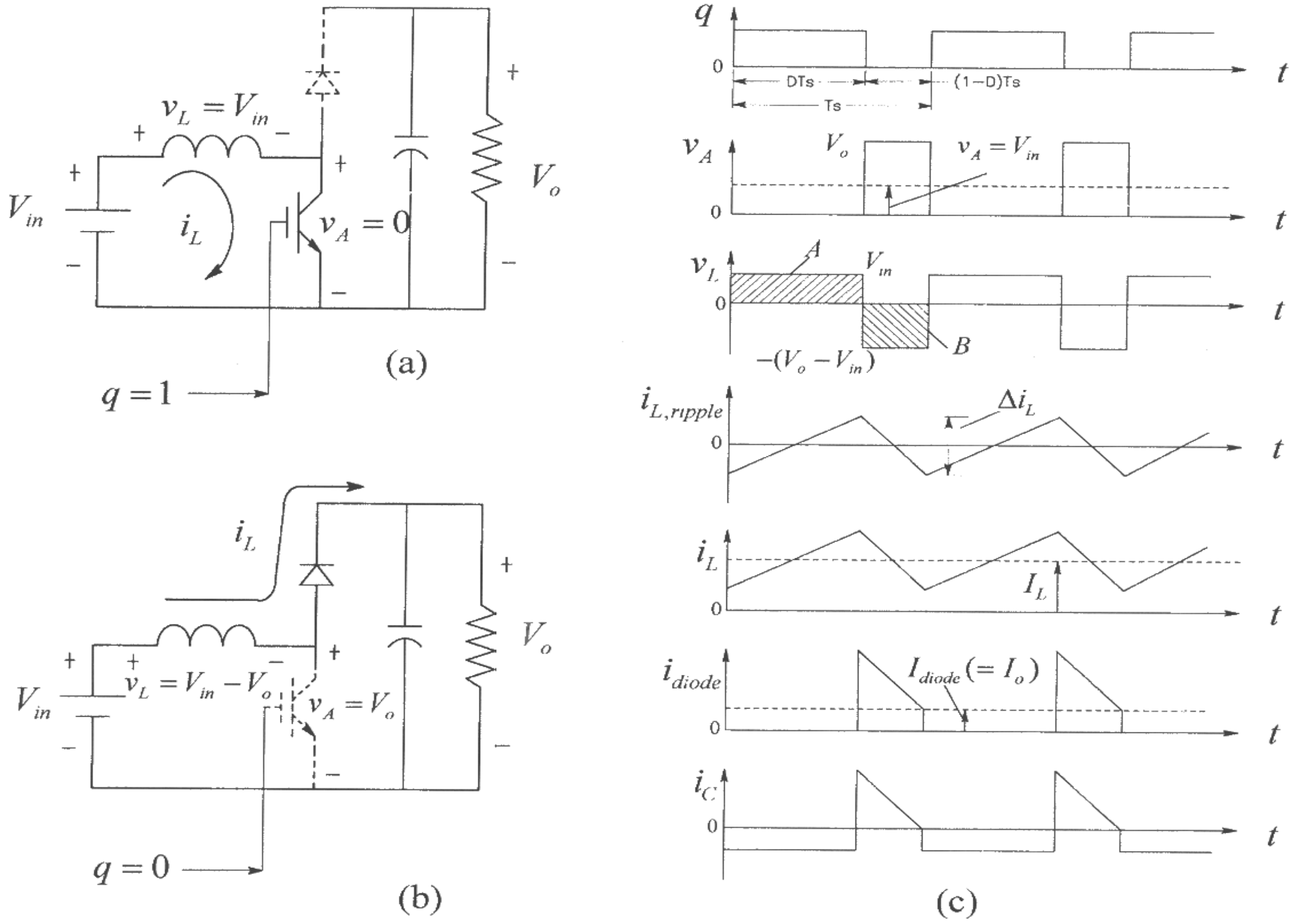


Figure 3-4 Boost dc-dc converter.

It is conventional to show power flow from the left to the right side. To follow this convention, the circuit of Fig. 3-4a is flipped and drawn in Fig. 3-4b. The output stage consists of the output load and a large filter capacitor that is used to minimize the output voltage ripple. This capacitor at the output initially gets charged to a voltage equal to V_{in} through the diode.

In a Boost converter, turning on the transistor in the bottom position applies the input voltage across the inductor such that v_L equals V_{in}, as shown in Fig. 3-5a, and i_L linearly ramps up, increasing the energy in the inductor. Turning off the transistor forces the inductor current to flow through the diode as shown in Fig. 3-5b, and some of the inductively stored energy is transferred to the output stage that consists of the filter capacitor and the output load across it.


$v_L = V_{in}$
+
−
+
V_{in}
−
i_L
+
$v_A = 0$
−
+
V_o
−
$q = 1$
i_L
+
+
$v_L = V_{in} - V_o$
−
V_{in}
−
+
$v_A = V_o$
−
+
V_o
−
$q = 0$
q
0
DTs
(1−D)Ts
Ts
t
v_A
V_o
$v_A = V_{in}$
0
t
v_L
A
V_{in}
0
$-(V_o - V_{in})$
B
t
$i_{L,ripple}$
Δi_L
0
t
i_L
I_L
0
t
i_{diode}
$I_{diode} (= I_o)$
0
t
i_C
0
t

(a) (b) (c)

Figure 3-5 Boost converter: operation and waveforms.

The transistor switching function is shown in Fig. 3-5c, with a steady state duty-ratio D. Because of the transistor in the bottom position in the power-pole, the resulting v_A waveform is as plotted in Fig. 3-5c. Since the average voltage across the inductor in the dc steady state is zero, the average voltage V_A equals the input voltage V_{in}. The inductor voltage v_L pulsates between two values: V_{in} and $-(V_o - V_{in})$ as plotted in Fig. 3-5c. Since the average inductor voltage is zero, the volt-second areas during the two sub-intervals are equal in magnitude and opposite in sign.

The input/output voltage ratio can be obtained either by the waveform of v_A or v_L in Fig. 3-5c. Using the inductor voltage waveform whose average is zero in dc steady state,

$$V_{in}(DT_s) = (V_o - V_{in})(1-D)T_s \tag{3-18}$$

Hence,

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \qquad (V_o > V_{in}) \tag{3-19}$$

The inductor current waveform consists of its average value, which depends on the output load, and a ripple component that depends on v_L:

$$i_L(t) = I_L + i_{L,ripple}(t) \tag{3-20}$$

where as shown in Fig. 3-5c, $i_{L,ripple}\left(= \frac{1}{L}\int v_L \cdot d\tau\right)$, whose average value is zero, consists of linear segments, rising when v_L is positive and falling when v_L is negative. The peak-peak ripple can be calculated by using either area *A* or *B*:

$$\Delta i_L = \frac{1}{L}\underbrace{V_{in}(DT_s)}_{\text{Area A}} = \frac{1}{L}\underbrace{(V_o - V_{in})(1-D)T_s}_{\text{Area B}} \tag{3-21}$$

In a Boost converter, the inductor current equals the input current, whose average can be calculated from the output load current by equating the input and the output powers:

$$V_{in}I_{in} = V_o I_o \tag{3-22}$$

Hence, using Eq. 3-19 and $I_o = V_o / R$,

$$I_L = I_{in} = \frac{V_o}{V_{in}} I_o = \frac{I_o}{1-D} = \frac{1}{1-D}\frac{V_o}{R} \tag{3-23}$$

The inductor current waveform is shown in Fig. 3-5c, superposing its average and the ripple components.

The current through the diode equals 0 when the transistor is on, otherwise it equals i_L, as plotted in Fig. 3-5c. In the dc steady state, the average capacitor current I_C is zero and therefore the average diode current equals the output current I_o. In practice, the filter capacitor is large to achieve the output voltage nearly dc $(v_o(t) \simeq V_o)$. Therefore, to the ripple-frequency component in the diode current, the path through the capacitor offers much smaller impedance than through the load resistance, hence justifies the assumption that the ripple component of the diode current flows entirely through the capacitor. That is,

$$i_C(t) \simeq i_{diode,ripple}(t) = i_{diode} - I_o \tag{3-24}$$

In practice, the voltage drops across the capacitor ESR and the ESL dominate over the voltage drop $\frac{1}{C}\int i_C dt$ across C. The plot of i_C in Fig. 3-5c can be used to calculate the ripple in the output voltage.

The above analysis shows that voltage conversion ratio (Eq. 3-19) of Boost converters in CCM depends on $1/(1-D)$, and is independent of the output load, as shown in Fig. 3-6. If the output load decreases to the extent that the inductor current becomes discontinuous below a critical value $I_{L,crit}$, the input-output relationship of CCM is no longer valid in DCM. If the duty-ratio D were to be held constant as shown in Fig. 3-6, the output voltage could rise to dangerously high levels in DCM, considered fully in section 3-15 and the Appendix to this chapter.

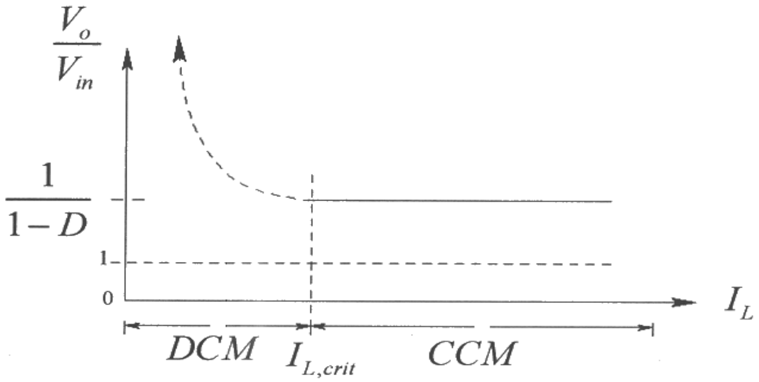
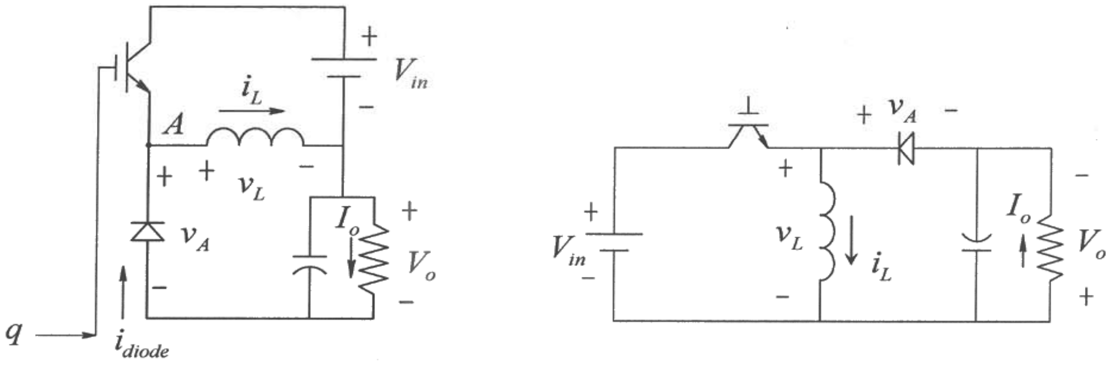


Figure 3-6 Boost converter: voltage transfer ratio.

3-7 BUCK-BOOST CONVERTER ANALYSIS IN DC STEADY STATE

Buck-Boost converters allow the output voltage to be greater or lower than the input voltage based on the switch duty-ratio D. A Buck-Boost converter is shown in Fig. 3-7a, where the switching power-pole is implemented as shown. Conventionally, to make the power flow from left to the right, the Buck-Boost converter is drawn as shown in Fig. 3-7b.

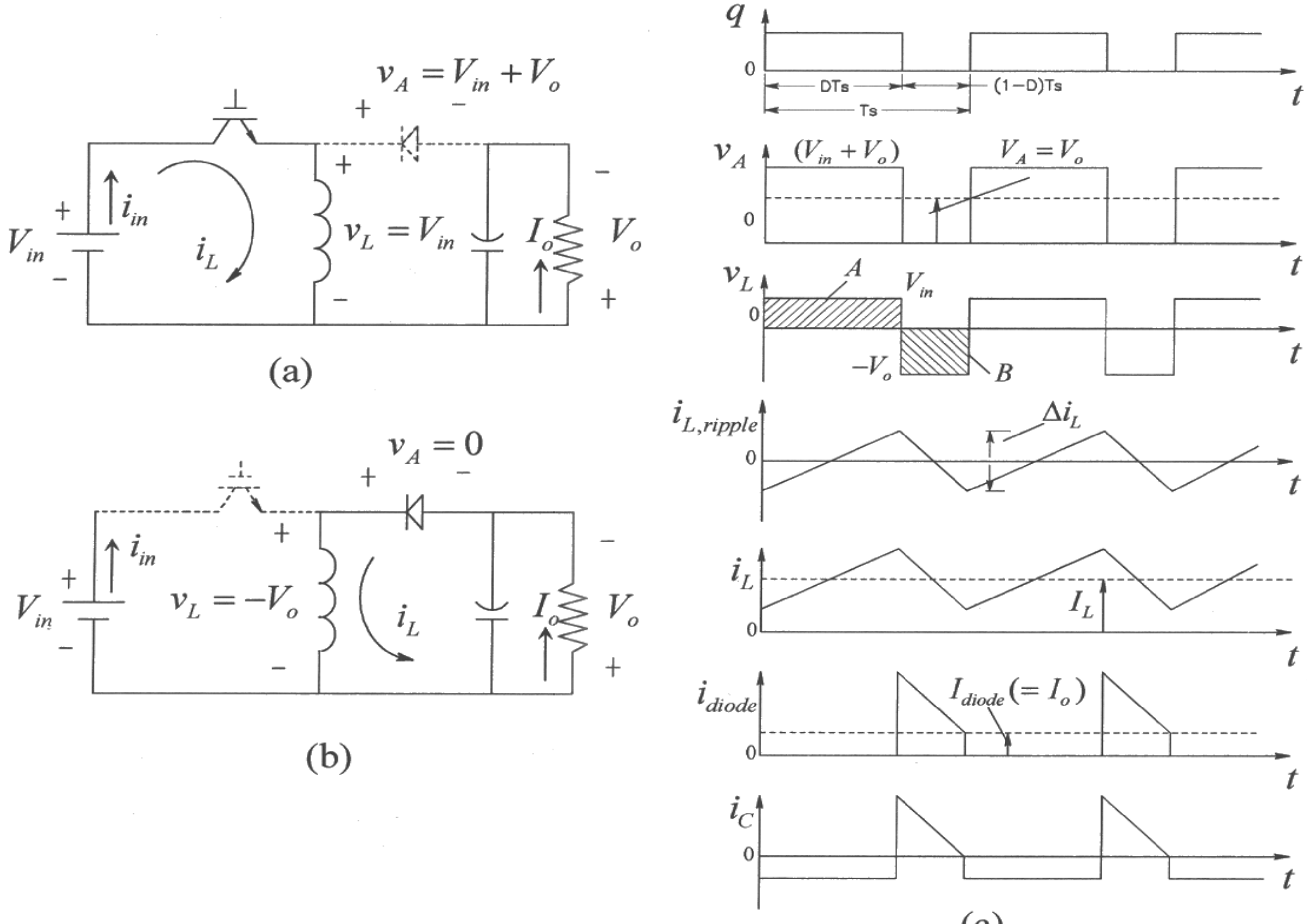
As shown in Fig. 3-8a, turning on the transistor applies the input voltage across the inductor such that v_L equals V_{in}, and the current linearly ramps up, increasing the energy in the inductor. Turning off the transistor results in the inductor current flowing through the diode, as shown in Fig. 3-8b, transferring energy increase in the inductor during the previous transistor state to the output.



V_{in}
i_L
A
v_L
v_A
I_o
V_o
i_{diode}
q
v_A
V_{in}
v_L
i_L
I_o
V_o

(a) (b)

Figure 3-7 Buck-Boost dc-dc converter.



$v_A = V_{in} + V_o$
i_{in}
V_{in}
i_L
$v_L = V_{in}$
I_o
V_o
(a)
$v_A = 0$
i_{in}
V_{in}
$v_L = -V_o$
i_L
I_o
V_o
(b)
q
DTs
(1−D)Ts
Ts
v_A
$(V_{in} + V_o)$
$V_A = V_o$
v_L
A
V_{in}
$-V_o$
B
$i_{L,ripple}$
Δi_L
i_L
I_L
i_{diode}
$I_{diode} (= I_o)$
i_C
0
t
(c)

Figure 3-8 Buck-Boost converter: operation and waveforms.

The transistor switching function is shown in Fig. 3-8c, with a steady state duty-ratio D. The resulting v_A waveform is as plotted. Since the average voltage across the inductor in the dc steady state is zero, the average V_A equals the output voltage. The inductor voltage pulsates between two values: V_{in} and $-V_o$, as plotted in Fig. 3-8c. Since the average inductor voltage is zero, the volt-second areas during the two sub-intervals are equal in magnitude and opposite in sign.

The input/output voltage ratio can be obtained either by the waveform of v_A or v_L in Fig. 3-8c. Using the v_L waveform whose average is zero in the dc steady state,

$$DV_{in} = (1-D)V_o \tag{3-25}$$

Hence,

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \tag{3-26}$$

The inductor current consists of an average value, which depends on the output load, and a ripple component that depends on v_L :

$$i_L(t) = I_L + i_{L,ripple}(t) \tag{3-27}$$

where as shown in Fig. 3-8b, $i_{L,ripple}\left(=\frac{1}{L}\int v_L \cdot d\tau\right)$, whose average value is zero, consists of linear segments, rising when v_L is positive and falling when v_L is negative. The peak-peak ripple can be calculated by using either area *A* or *B*

$$\Delta i_L = \frac{1}{L}\underbrace{V_{in}(DT_s)}_{\text{Area A}} = \frac{1}{L}\underbrace{V_o(1-D)T_s}_{\text{Area B}} \tag{3-28}$$

Applying the Kirchhoff's current law in Fig. 3-7a or b, the average inductor current equals the sum of the average input current and the average output current (note that the average capacitor current is zero in dc steady state)

$$I_L = I_{in} + I_o \tag{3-29}$$

Equating the input and the output powers

$$V_{in}I_{in} = V_oI_o \tag{3-30}$$

and using Eq. 3-26

$$I_{in} = \frac{V_o}{V_{in}}I_o = \frac{D}{1-D}I_o \tag{3-31}$$

Hence, using Eqs. 3-29 and 3-31,

$$I_L = I_{in} + I_o = \frac{1}{1-D}I_o = \frac{1}{1-D}\frac{V_o}{R} \tag{3-32}$$

Superposing the average and the ripple components, the inductor current waveform is shown in Fig. 3-8c.

The diode current is zero, except when it conducts the inductor current, as plotted in Fig. 3-8c. In the dc steady state, the average current I_C through the capacitor is zero, and therefore by the Kirchhoff's current law, the average diode current equals the output current. In practice, the filter capacitor is large to achieve the output voltage nearly dc $(v_o(t) \simeq V_o)$. Therefore, to the ripple-frequency current, the path through the capacitor offers much smaller impedance than through the load resistance, hence justifies the assumption that the ripple component of the diode current flows entirely through the capacitor. That is,

$$i_C(t) \simeq i_{diode,ripple}(t) \tag{3-33}$$

In practice, the voltage drops across the capacitor ESR and the ESL dominate over the voltage drop $\frac{1}{C}\int i_C dt$ across C. The plot of i_C in Fig. 3-8c can be used to calculate the ripple in the output voltage.

The above analysis shows that the voltage conversion ratio (Eq. 3-26) of Buck-Boost converters in CCM depends on $D/(1-D)$, and is independent of the output load, as shown in Fig. 3-9. If the output load decreases to the extent that the inductor current becomes discontinuous below a critical value $I_{L,crit}$, the input-output relationship in CCM is no longer valid in DCM. If the duty-ratio D were to be held constant as shown in Fig. 3-9, the output voltage could rise to dangerously high levels in DCM, considered fully in section 3-15 and the Appendix to this chapter.

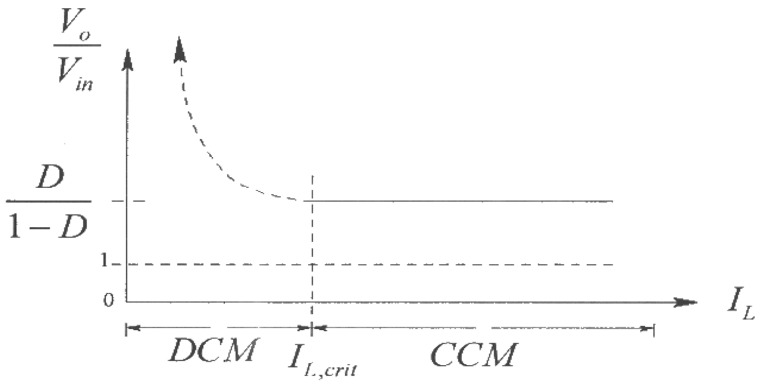


Figure 3-9 Buck-Boost converter: voltage transfer ratio.

3-7-1 Other Buck-Boost Topologies

There are two variations of the Buck-Boost topology, which are used in certain applications. These two topologies are briefly described below.

3-7-1-1 SEPIC Converters (Single-Ended Primary Inductor Converters)

The SEPIC converter shown in Fig. 3-10a is used in certain applications where the current drawn from the input is required to be relatively ripple-free. By applying the Kirchhoff's voltage law and the fact that average inductor voltage is zero in the dc steady state, the capacitor in this converter gets charged to an average value that equals the input voltage V_{in} with the polarity shown. During the on-interval of the transistor, DT_s, as shown in Fig. 3-10b, the diode gets reverse biased by the sum of the capacitor and the output voltages, and i_{L1} and i_{L2} flow through the transistor. During the off-interval $(1-D)T_s$, i_{L1} and i_{L2} flow through the diode, as shown in Fig. 3-10c. The voltage across L_2 equals v_C during the on-interval, and equals $(-V_o)$ during the off-interval. In terms of the average value of the capacitor voltage that equals V_{in} (by applying Eq. 3-9 in Fig. 3-10a), equating the average voltage across L_2 to zero results in

$$DV_{in} = (1-D)V_o \tag{3-34}$$

or,

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \tag{3-35}$$

Unlike the Buck-Boost converters, the output voltage polarity in SEPIC converter remains the same as that of the input.

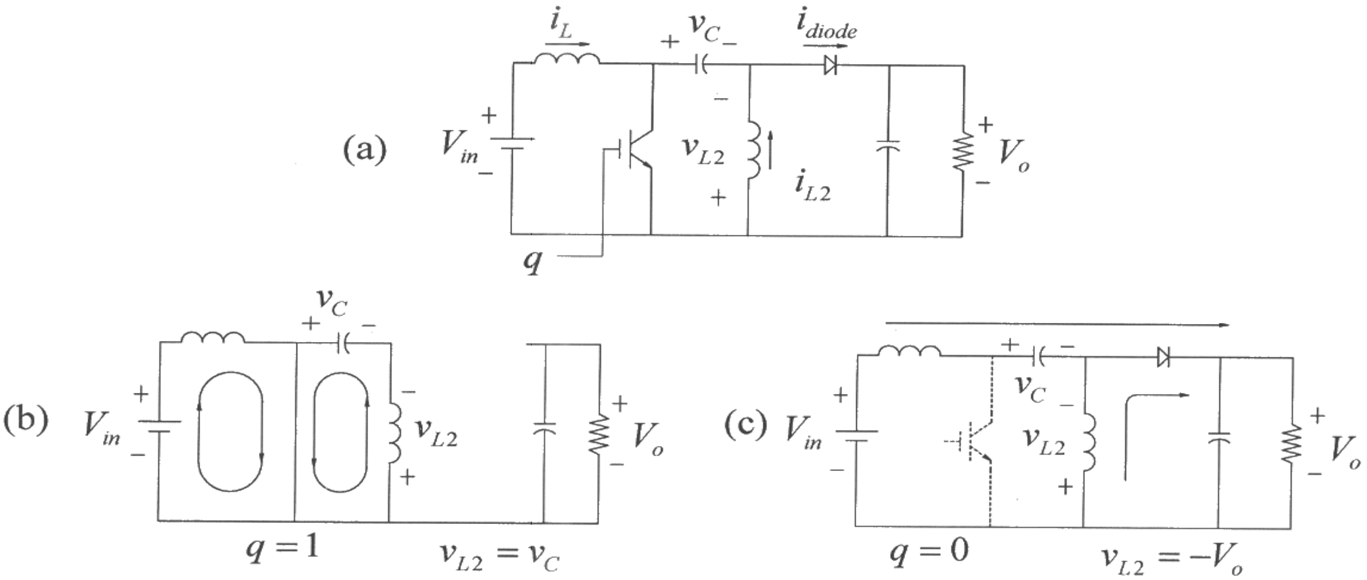


Figure 3-10 SEPIC converter.

3-7-1-2 Cuk Converter

Named after its inventor, the Cuk converter is as shown in Fig. 3-11a, where the energy transfer means is through the capacitor C between the two inductors. Using Eq. 3-9 in Fig. 3-11a, this capacitor voltage has an average value of $(V_{in} + V_o)$ with the polarity shown. During the on-interval of the transistor, DT_s, as shown in Fig. 3-11b, the diode gets reverse biased by the capacitor voltage and the input and the output currents flow through the transistor. During the off-interval $(1-D)T_s$, the input and the output currents flow through the diode, as shown in Fig. 3-11c. In terms of the average values of the inductor currents, equating the net change in charge on the capacitor over T_s to zero in steady state,

$$DI_o = (1-D)I_{in} \tag{3-36}$$

or

$$\frac{I_{in}}{I_o} = \frac{D}{1-D} \tag{3-37}$$

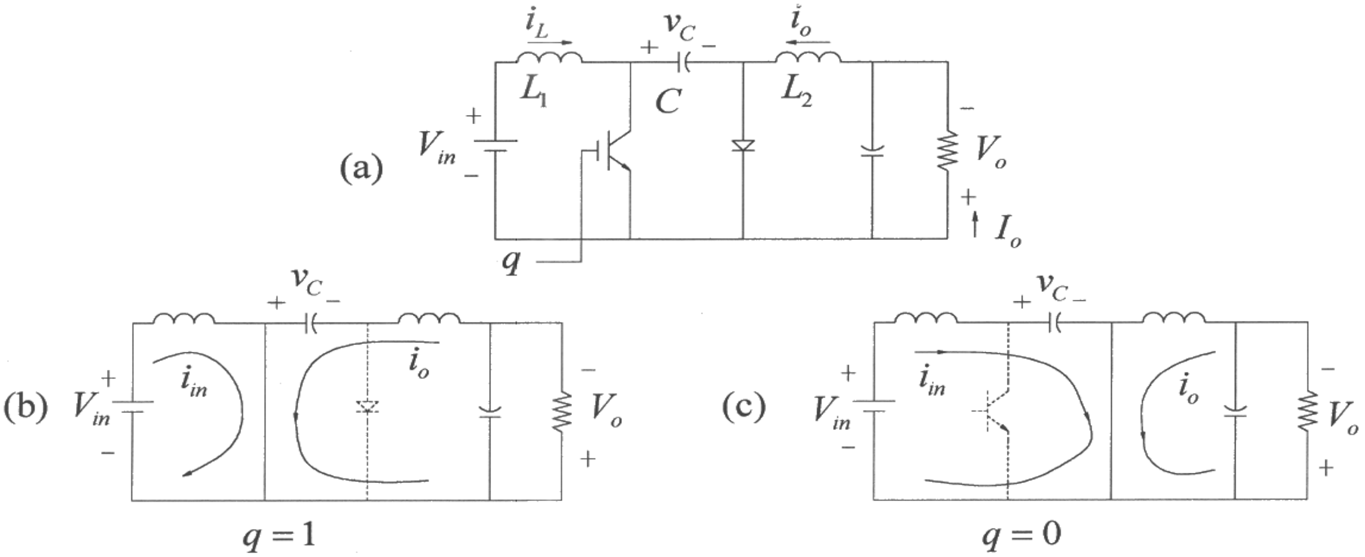


Figure 3-11 Cuk converter.

Equating input and output powers in this idealized converter leads to

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \tag{3-38}$$

which shows the same functionality as Buck-Boost converters. One of the advantages of the Cuk converter is that it has non-pulsating currents at the input and the output but it suffers from the same component stress disadvantages as the Buck-Boost converters and produces an output voltage of the polarity opposite to that of the input.

3-8 TOPOLOGY SELECTION [2]

For selecting between the three converter topologies discussed in this chapter, the stresses listed in Table 3-1 can be compared, which are based on the assumption that the inductor ripple current is negligible.

Table 3-1 Topology Selection Criteria

Criterion		Buck	Boost	Buck-Boost
Transistor $\hat{V}$		V_{in}	V_o	$(V_{in}+V_o)$
Transistor $\hat{I}$		I_o	I_{in}	$I_{in}+I_o$
I_{rms}	Transistor	$\sqrt{D}I_o$	$\sqrt{D}I_{in}$	$\sqrt{D}\left(I_{in}+I_o\right)$
I_{avg}	Transistor	DI_o	DI_{in}	$D\left(I_{in}+I_o\right)$
	Diode	$(1-D)I_o$	$(1-D)I_{in}$	$(1-D)\left(I_{in}+I_o\right)$
I_L		I_o	I_{in}	$I_{in}+I_o$
Effect of L on C		significant	little	little
Pulsating Current		input	output	both

From the above table, we can clearly conclude that the Buck-Boost converter suffers from several additional stresses. Therefore, it should be used only if both the Buck and the Boost capabilities are needed. Otherwise, the Buck or the Boost converter should be used based on the desired capability. A detailed analysis is carried out in [2].

3-9 WORST-CASE DESIGN

The worst-case design should consider the ranges in which the input voltage and the output load vary. As mentioned earlier, often converters above a few tens of watts are designed to operate in CCM. To ensure CCM even under very light load conditions would require prohibitively large inductance. Hence, the inductance value chosen is often no larger than three times the critical inductance $\left(L<3L_c\right)$, where, as discussed in section 3-15, the critical inductance L_c is the value of the inductor that will make the converter operate at the border of CCM and DCM at full-load.

3-10 SYNCHRONOUS-RECTIFIED BUCK CONVERTER FOR VERY LOW OUTPUT VOLTAGES [3]

Operating voltages in computing and communication equipment have already dropped to an order of 1 V and even lower voltages, such as 0.5 V, are predicted in the near future.

At these low voltages, the diode (even a Schottky diode) of the power-pole in a Buck converter has unacceptably high voltage drop across it in comparison to the output voltage, resulting in extremely poor converter efficiency.

As a solution to this problem, the switching power-pole in a Buck converter is implemented using two MOSFETs, as shown in Fig. 3-12a, which are available with very low $R_{DS(on)}$ in low voltage ratings. The two MOSFETs are driven by almost complimentary gate signals (some delay time, where both signals are low is necessary to avoid the shoot-through of current through the two transistors), as shown in Fig. 3-12b. When the upper MOSFET is off, the inductor current flows through the channel, from the source to the drain, of the lower MOSFET that has gate voltage applied to it. This results in a very low voltage drop across the lower MOSFET. At light load conditions, the inductor current may be allowed to become negative without becoming discontinuous, flowing from the drain to the source of the lower MOSFET [3].

It is possible to achieve soft-switching in such converters, as discussed in Chapter 10, where the ripple in the total output and the input currents can be minimized by interleaving which is discussed in the next section.

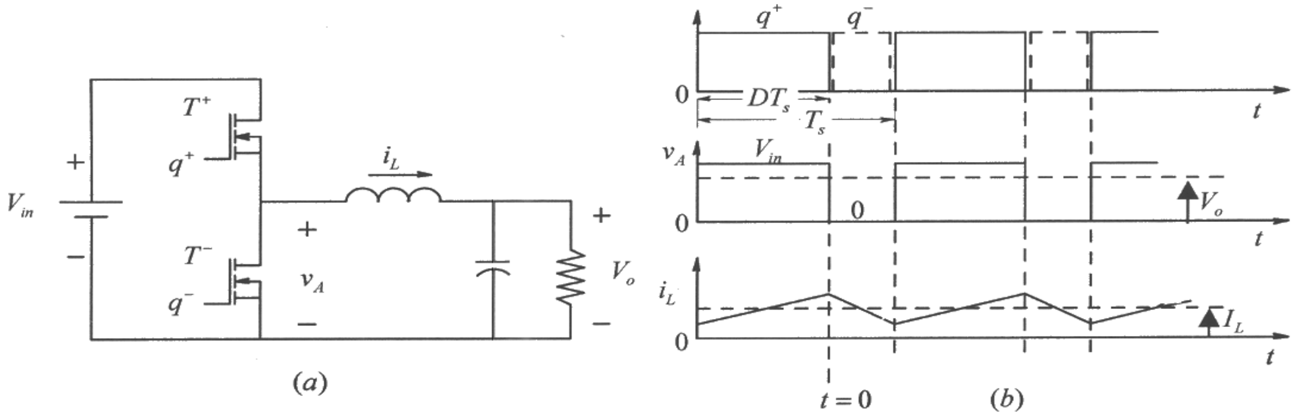


Figure 3-12 Buck converter: synchronous rectified.

3-11 INTERLEAVING OF CONVERTERS [4]

Fig. 3-13a shows two interleaved converters whose switching waveforms are phase shifted by $T_s/2$, as shown in Fig. 3-13b. In general, n such converters can be used, their operation phase shifted by T_s/n. The advantage of such interleaved multi-phase converters is the cancellation of ripple in the input and the output currents to a large degree [4]. This is also a good way to achieve higher control bandwidth.

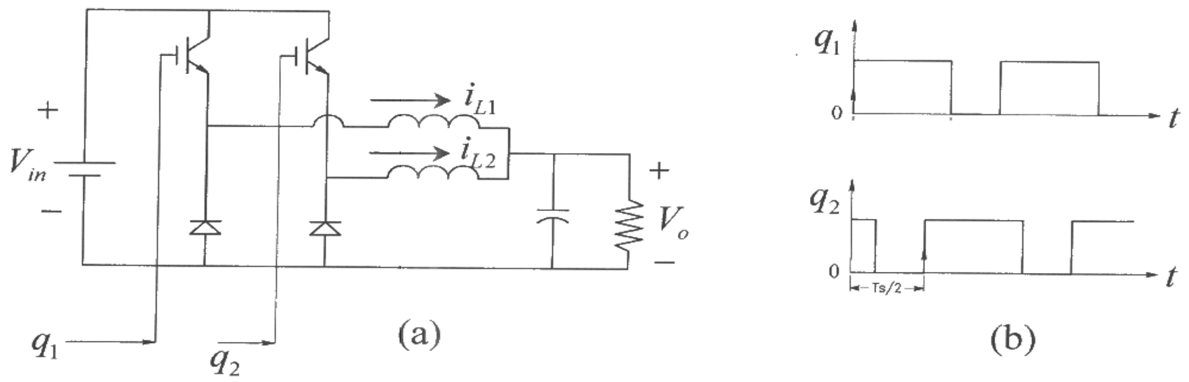


Figure 3-13 Interleaving of converters.

3-12 REGULATION OF DC-DC CONVERTERS BY PWM

Almost all dc-dc converters are operated with their output voltages regulated to equal their reference values within a specified tolerance band (for example, ± 1 % around its nominal value) in response to disturbances in the input voltage and the output load. The average output of the switching power-pole in a dc-dc converter can be controlled by pulsed-width-modulating (PWM) the duty-ratio $d(t)$ of this power-pole. Fig. 3-14a shows in a block-diagram form of a regulated dc-dc converter. It shows that the converter output voltage is measured and compared with its reference value within a PWM controller IC [5], briefly described in Chapter 2. The error between the two voltages is amplified by an amplifier, whose output is the control voltage $v_c(t)$.

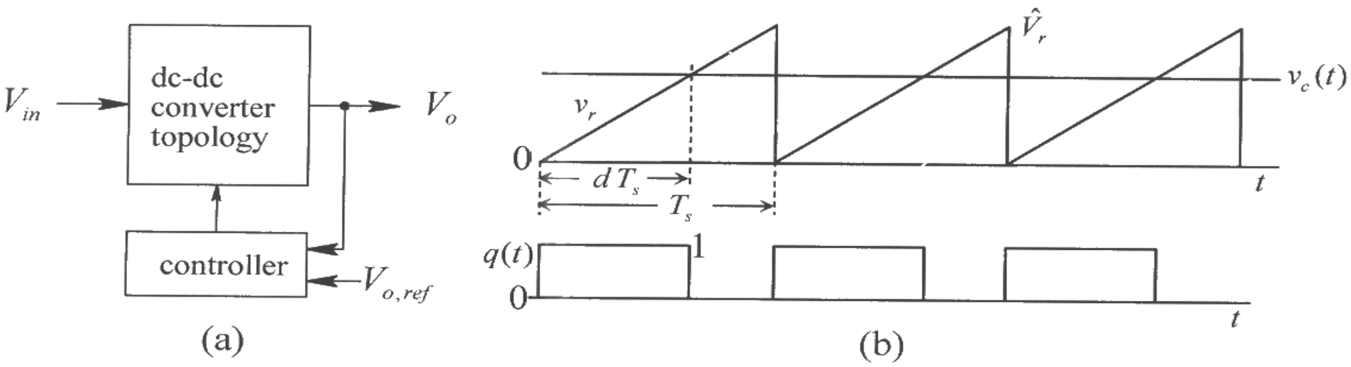


Figure 3-14 Regulation of output by PWM.

Within the PWM-IC [5], the control voltage is compared with a ramp signal $v_r(t)$ as shown in Fig. 3-14b, where the comparator output represents the switching function $q(t)$ whose pulse-width $d(t)$ can be modulated to regulate the output of the converter. The ramp signal v_r has the amplitude $\hat{V}_r$, and the switching frequency f_s constant. The output voltage of this comparator represents the transistor switching function $q(t)$, which equals 1 if $v_c(t) \geq v_r$; otherwise 0. The switch duty-ratio in Fig. 3-14b is given as

$$d(t) = \frac{v_c(t)}{\hat{V}_r} \qquad (3\text{-}39)$$

thus the control voltage, limited in a range between 0 and $\hat{V}_r$, linearly and dynamically controls the pulse-width $d(t)$ in Eq. 3-39 and shown in Fig. 3-14b.

3-13 DYNAMIC AVERAGE REPRESENTATION OF CONVERTERS IN CCM

In all three types of dc-dc converters in CCM, the switching power-pole switches between two sub-circuit states based on the switching function $q(t)$. (It switches between three sub-circuit states in DCM, where the switch can be considered "Stuck" between the on and the off positions during the subinterval when the inductor current is zero, discussed in detail in the Appendix.) It is very beneficial to obtain non-switching average models of these switch-mode converters for simulating the converter performance under dynamic conditions caused by the change of input voltage and/or the output load. Under the dynamic condition, the converter duty-ratio, and the average values of voltages and currents within the converter vary with time, but relatively slowly with frequencies an order of magnitude smaller than the switching frequency.

The switching power-pole is shown in Fig. 3-15a, where the voltages and currents are labeled with the subscript *vp* for the voltage-port and *cp* for the current-port. In the above analysis for the three converters in the dc steady state, we can write the average voltage and current relationships for the bi-positional switch of the power-pole as

$$V_{cp} = DV_{vp} \qquad (3\text{-}40a)$$

$$I_{vp} = DI_o \qquad (3\text{-}40b)$$

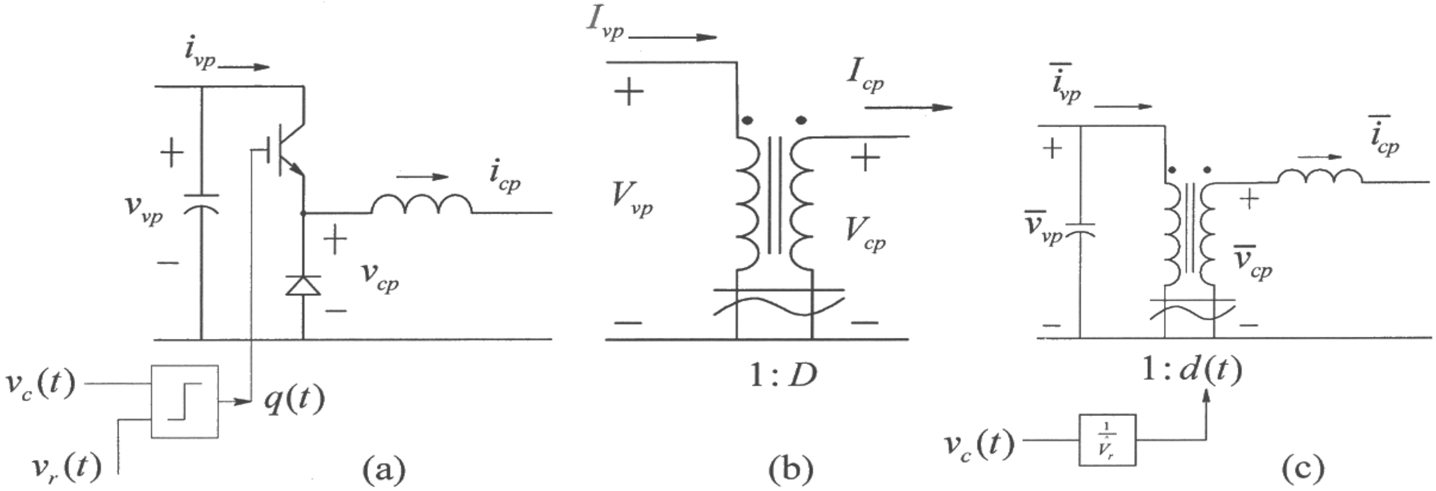


Figure 3-15 Average dynamic model of a switching power-pole.

Relationships in Eq. 3-40 can be represented by an ideal transformer as shown in Fig. 3-15b. Under dynamic conditions, the average model in Fig. 3-15b of the bi-positional switch can be substituted in the power-pole of Fig. 3-15a, resulting in the dynamic average model shown in Fig. 3-15c, using Eq. 3-39 for $d(t)$. Here, the uppercase letters used in the dc steady state relationships are replaced with lowercase letters with a "-" on top to represent average voltages and currents, which may vary dynamically with time: D by $d(t)$, V_{cp} by $\overline{v}_{cp}(t)$, I_{cp} by $\overline{i}_{cp}(t)$, and I_{vp} by $\overline{i}_{vp}(t)$. Therefore, from Eqs. 3-40a and b:

$$\overline{v}_{cp}(t) = d(t)\overline{v}_{vp}(t) \tag{3-41a}$$

$$\overline{i}_{vp}(t) = d(t)\overline{i}_{cp}(t) \tag{3-41b}$$

The above discussion shows that the dynamic average model of a switching power-pole in CCM is an ideal transformer with the turns-ratio $1:d(t)$. Using this model for the switching power-pole, the dynamic average models of the three converters shown in Fig. 3-16a are as in Figs. 3-16b in CCM. Note that in the Boost converter where the transistor is in the bottom position in the power-pole, the transformer turn-ratio is $1:(1-d)$, because the pole duty-ratio d_A is 1 minus the transistor duty-ratio $d(t)$. The average representation of these converters in DCM is described in the Appendix.

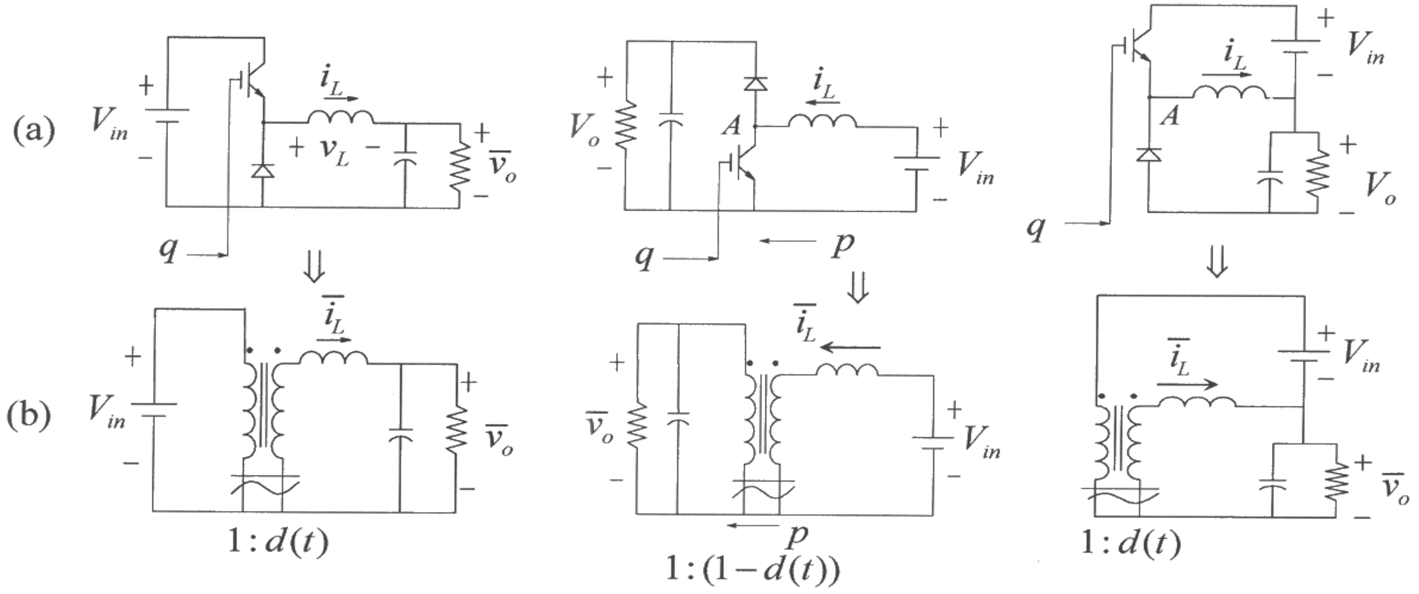


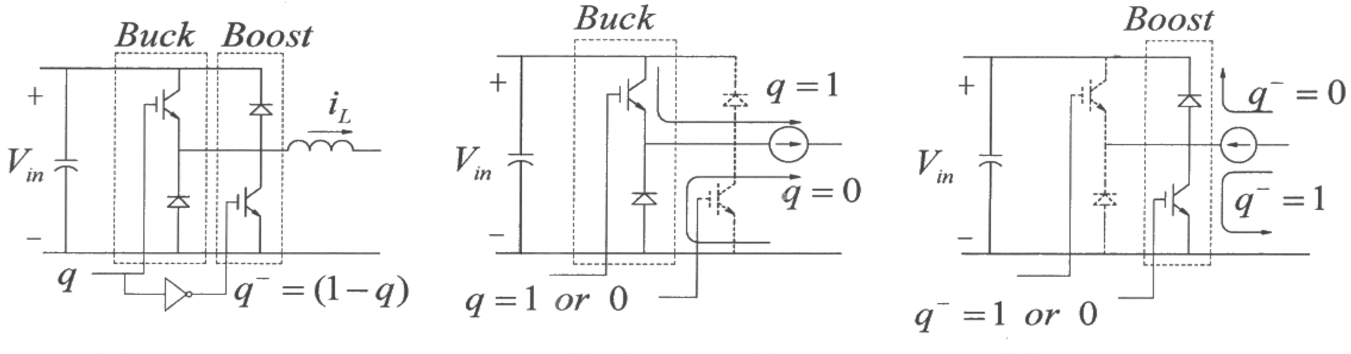
Figure 3-16 Average dynamic models of three converters.

The ideal transformers in the circuits of Fig. 3-16b, being hypothetical and only a convenience for mathematical representation, can operate with ac as well dc voltages and currents, which a real transformer cannot. A symbol consisting of a straight bar with a curve below is used to remind us of this fact. Since no electrical isolation exists between the voltage-port and the current-port of the switching power-pole, the two windings in the circuits of Fig. 3-15c and Fig. 3-16b are connected at the bottom. Moreover, the voltages in the circuit of Fig. 3-16 cannot become negative (however, depending on the implementation of the power-pole, the currents may become negative, that is, reverse directions), and d is limited to a range between 0 to 1.

In the average representation of the switching power-pole, all the switching information is removed, and hence it provides an uncluttered understanding of achieving desired objectives in various converters. Moreover, the average model in simulating the dynamic response of a converter results in computation speeds orders of magnitude faster than that in the switching model, where the simulation time step must be smaller than at least one-hundredth of the switching time-period T_s in order to achieve an accurate resolution.

3-14 BI-DIRECTIONAL SWITCHING POWER-POLE

In Buck, Boost and Buck-Boost dc-dc converters, the implementation of the switching power-pole by one transistor and one diode dictates the instantaneous current flow to be unidirectional. As shown in Fig. 3-17a, by combining the switching power-pole implementations of Buck and Boost converters, where the two transistors are switched by complimentary signals, allows a continuous bi-directional power and current capability. In such a bi-directional switching power-pole, the positive inductor current as shown in Fig. 3-17b represents a Buck mode, where only the transistor and the diode associated with the Buck converter take part. Similarly, as shown in Fig. 3-17c, the negative inductor current represents a Boost mode, where only the transistor and the diode associated with the Boost converter take part. We will utilize such bi-directional switching power-poles in dc and ac motor drives discussed in Chapters 11 and 12.



(a) (b) i_L = positive (c) i_L = negative

Figure 3-17 Bi-directional power flow through a switching power-pole.

In a bi-directional switching power-pole where the transistors are gated by complimentary signals, the current through it can flow in either direction, and hence ideally, a discontinuous conduction mode does not exist. The average representation of the bi-directional switching power-pole in Fig. 3-18a is an ideal transformer shown in Fig. 3-18b with a turns-ratio $1:d(t)$, where $d(t)$ represents the pole duty-ratio that is also the duty-ratio of the transistor associated with the Buck mode.

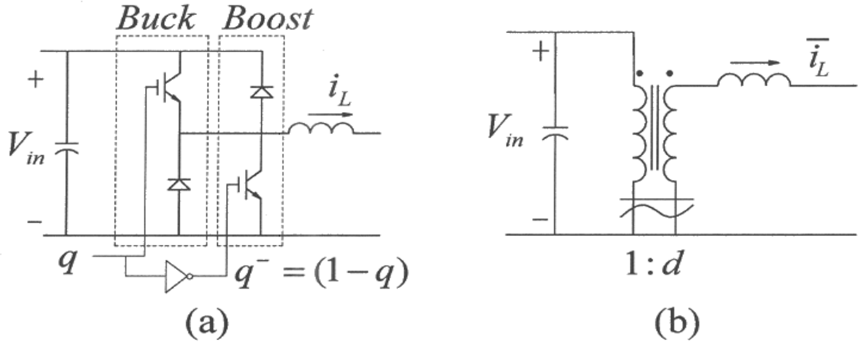


Figure 3-18 Average dynamic model of the switching power-pole with bi-directional power flow.

3-15 DISCONTINUOUS-CONDUCTION MODE (DCM)

All dc-dc converters for unidirectional power and current flow have their switching power-pole implemented by one transistor and one diode, and hence go into a discontinuous conduction mode, DCM, below a certain output load. This operating mode for all three converters is examined in detail in the Appendix, whereas only the critical loads above which converters operate in CCM are examined here.

As an example as shown in Fig. 3-19, if we keep the switch duty-ratio constant, decline in the output load results in the inductor average current to decrease until a critical load value is reached where the inductor current waveform reaches zero at the end of the turn-off interval. The average inductor current in this condition, we will call the critical inductor current, $I_{L,crit}$. For loads below this critical value, the inductor current cannot reverse through the diode in any of the three converters (Buck, Boost and Buck-Boost), and enters DCM where the inductor current remains zero for a finite interval.

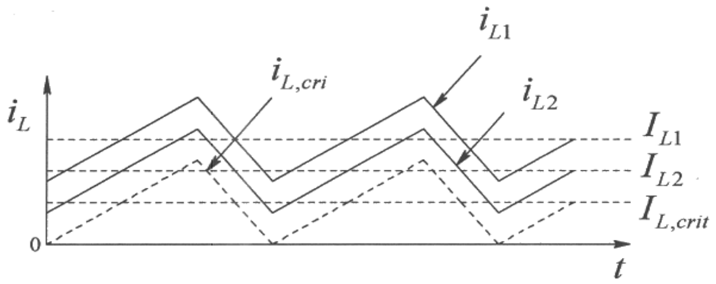


Figure 3-19 Inductor current at various loads; duty-ratio is kept constant.

In DCM, the inductor current conduction becomes discontinuous for an interval during which there is no power drawn from the input source and there is no energy in the inductor to transfer to the output stage. This interval of inactivity during which the inductor current remains zero generally results in increased device stresses and the ratings of the passive components. DCM also results in noise and EMI, although the diode reverse recovery problem is minimized. Based on these considerations, converters above a few tens of watts are generally designed to operate in CCM, although all of them implemented using one transistor and one diode will enter DCM at very light loads and the feedback controller should be designed to operate adequately in both modes. It should be noted that designing the controller of some converters, such as the Buck-Boost converters, in CCM is much more complicated, thus the designers may prefer to keep such converters in DCM for all possible operating conditions. This we will discuss further in the next chapter dealing with the feedback controller design.

The inductor current at the critical average value, although at the border of CCM and DCM, should be considered to belong to the CCM case. At this critical load condition, the inductor voltage v_L and the current i_L are drawn in Fig. 3-20a-c for the three converters shown in Figs. 3-3a, 3-4a and 3-7a. As can be seen from the i_L waveform in these critical cases in Fig. 3-20, the average inductor current is one-half the peak-peak ripple.

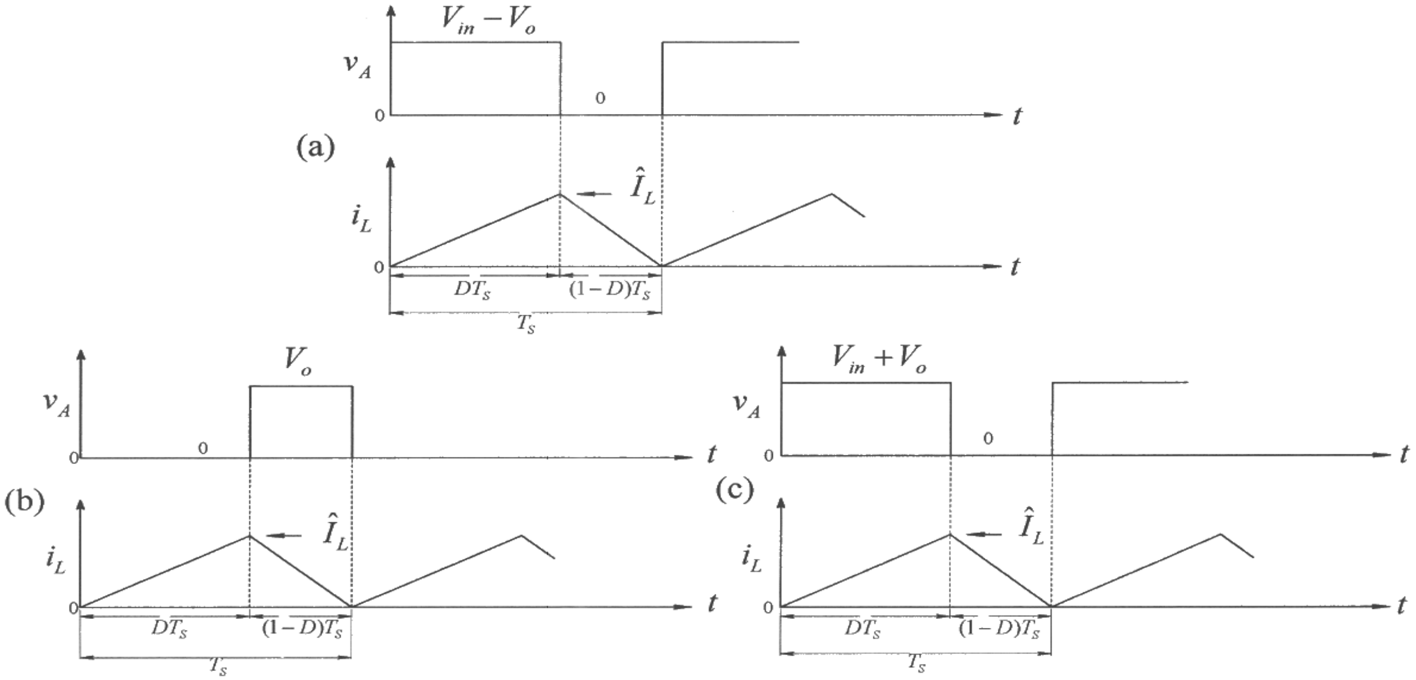


Figure 3-20 Waveforms for the three converters at the border of CCM/DCM.

In the Buck converter of Fig. 3-3a, the peak inductor current in Fig. 3-20a can be calculated by the fact that a voltage ($V_{in} - V_o$) is applied across the inductor for an interval

DT_s interval when the transistor is on, causing the current to rise from zero to its peak value. Therefore, the peak current is

$$\hat{I}_{L,crit,Buck} = \frac{(V_{in} - V_o)}{L} DT_s \tag{3-42}$$

With $f_s = 1/T_s$, and $V_o = DV_{in}$, the average current is

$$I_{L,crit,Buck} = \frac{V_{in}}{2Lf_s} D(1-D) \tag{3-43}$$

In both the Boost and the Buck-Boost converters, V_{in} is applied across the inductor for an interval DT_s interval when the transistor is on, causing the current to rise from zero to its peak value in Figs. 3-20b and c, respectively. Since the average inductor current is one-half of the peak value in these waveforms, the critical value is as follows:

$$I_{L,crit,Boost} = I_{L,crit,Buck\text{-}Boost} = \frac{V_{in}}{2Lf_s} D \tag{3-44}$$

If the average inductor current falls below its critical value in a converter, then its operation enters the DCM mode, which is discussed in detail in the Appendix.

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PROBLEMS

Buck DC-DC Converters

In a Buck dc-dc converter, $L = 50\,\mu H$. It is operating in dc steady state under the following conditions: $V_{in} = 40V$, $D = 0.3$, $P_o = 24W$, and $f_s = 200\,kHz$. Assume ideal components.

3-1 Calculate and draw the waveforms as shown in Fig. 3-3d.

3-2 Draw the inductor voltage and current waveforms if $P_o = 12W$; all else is unchanged. Compare the ripple in the inductor current with that in Problem 3-1.

3-3 In this Buck converter, the output load is changing. Calculate the critical value of the output load P_o below which the converter will enter the discontinuous conduction mode of operation.

3-4 Calculate the critical value of the inductance L below which this Buck converter will enter the discontinuous conduction mode at $P_o = 5W$ under all input voltage values.

3-5 Draw the waveforms for the variables shown in Fig. 3-3d for this Buck converter at the output load that causes it to operate at the border of continuous and discontinuous modes.

3-6 In this Buck converter, the input voltage is varying in a range from 24 V to 50 V. For each input value, the duty-ratio is adjusted to keep the output voltage constant at its nominal value (with $V_{in} = 40V$ and $D = 0.3$). Calculate the minimum value of the inductance L that will keep the converter in the continuous conduction mode at $P_o = 5W$.

Boost DC-DC Converters

In a Boost converter, $L = 50\,\mu H$. It is operating in dc steady state under the following conditions: $V_{in} = 12V$, $D = 0.4$, $P_o = 30W$, and $f_s = 200\,kHz$. Assume ideal components.

3-7 Calculate and draw and the waveforms as shown in Fig. 3-5c.

3-8 Draw the inductor voltage and current waveforms, if $P_o = 15W$; all else is unchanged. Compare the ripple in the inductor current with that in Problem 3-7.

3-9 In this Boost converter, the output load is changing. Calculate the critical value of the output load P_o below which the converter will enter the discontinuous conduction mode of operation.

3-10 Calculate the critical value of the inductance L below which this Boost converter will enter the discontinuous conduction mode of operation at $P_o = 5W$.

3-11 Draw the waveforms for the variables in Fig. 3-5c for this Boost converter at the output load that causes it to operate at the border of continuous and discontinuous modes.

3-12 In this Boost converter, the input voltage is varying in a range from 9 V to 15 V. For each input value, the duty-ratio is adjusted to keep the output voltage constant at its nominal value (with $V_{in} = 12V$ and $D = 0.4$). Calculate the minimum value of the inductance L that will keep the converter in the continuous conduction mode at $P_o = 5W$ under all input voltage values.

Buck-Boost DC-DC Converters

In a Buck-Boost converter, $L = 50\,\mu H$. It is operating in dc steady state under the following conditions: $V_{in} = 12V$, $D = 0.6$, $P_o = 36W$, and $f_s = 200kHz$. Assume ideal components.

3-13 Calculate and draw the waveforms as shown in Fig. 3-8c.

3-14 Draw the inductor voltage and current waveforms if $P_o = 18W$; all else is unchanged. Compare the ripple in the inductor current with that in Problem 3-13.

3-15 In this Buck-Boost converter, the output load is changing. Calculate the critical value of the output load P_o below which the converter will enter the discontinuous conduction mode of operation.

3-16 Calculate the critical value of the inductance L below which this Buck-Boost converter will enter the discontinuous conduction mode of operation at $P_o = 5W$.

3-17 Draw the waveforms for the variables in Fig. 3-8c for this Buck-Boost converter at the output load that causes it to operate at the border of continuous and discontinuous modes.

3-18 In this Buck-Boost converter, the input voltage is varying in a range from 9 V to 15 V. For each input value, the duty-ratio is adjusted to keep the output voltage constant at its nominal value (with $V_{in} = 12V$ and $D = 0.6$). Calculate the minimum value of the inductance L that will keep the converter in the continuous conduction mode of operation at $P_o = 5W$ under all input voltage values.

SEPIC DC-DC Converters

3-19 In a SEPIC converter, assume the ripple in the inductor currents and the capacitor voltage to be zero. This SEPIC converter is operating in a dc steady state under the following conditions: $V_{in} = 10V$, $D = 0.333$, $P_o = 50W$, and $f_s = 200kHz$. Assume ideal components. Draw the waveforms for all the converter variables under this dc steady-state condition.

Cuk DC-DC Converters

3-20 In a Cuk converter, assume the ripple in the inductor currents and the capacitor voltage to be zero. This Cuk converter is operating in a dc steady state under the following conditions: $V_{in} = 10V$, $D = 0.333$, $P_o = 50W$, and $f_s = 200kHz$. Assume ideal components. Draw the waveforms for all the converter variables under this dc steady-state condition.

Interleaving of DC-DC Converters

3-21 Two interleaved Buck converters, each similar to the Buck converter defined earlier before Problem 3-1, are supplying a total of $48W$. Calculate and draw the waveforms of the total input current and the total current $(i_{L_1} + i_{L_2})$ to the output stage. The gate signals to the converters are phase shifted by 180^0.

Regulation by PWM

3-22 In a Buck converter, consider two values of duty-ratios: 0.3 and 0.4. The switching frequency f_s is 200kHz and $\hat{V}_r = 1.2V$. Draw the waveforms as in Fig 3-14b.

Dynamic Average Models in CCM

3-23 Draw the dynamic average representations for Buck, Boost, Buck-Boost, SEPIC and Cuk Converters in the continuous conduction mode.

3-24 In the converters based on average representations in Problem 3-23, calculate the average input current for each converter in terms of the output current and the duty-ratio $d(t)$.

Bi-directional Switching Power-Poles

3-25 The dc-dc bi-directional converter of Fig. 3-18a interfaces a 12/14-V battery with a 36/42-V battery bank. The internal emfs are $E_1 = 40V$ (dc) and $E_2 = 13V$ (dc). Both these battery sources have an internal resistance of 0.1Ω each. In the dc steady state, calculate the power-pole duty-ratio D_A if (a) the power into the low-voltage battery terminals is 140 W, and (b) the power out of the low-voltage battery terminals is 140 W.

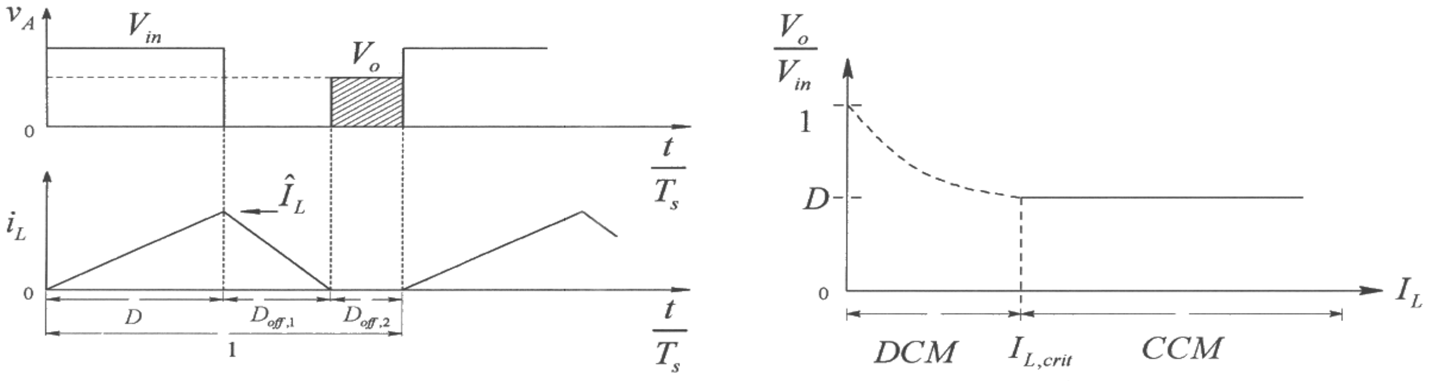
APPENDIX 3A DISCONTINUOUS-CONDUCTION MODE (DCM) IN DC-DC CONVERTERS

As briefly discussed earlier in section 3-15, all dc-dc converters for unidirectional power and current flow (implemented using one transistor and one diode) enter a discontinuous conduction mode, DCM, below a certain output load. The inductor current critical values at the border of CCM and DCM were derived for the three converters, and are given by Eq. 3-43 in Buck converters, and by Eq. 3-44 in both the Boost and the Buck-Boost converters.

3A-1 OUTPUT VOLTAGES IN DCM

3A-1-1 Buck Converters in DCM

For the Buck converter in Fig. 3-3a, an output load less than the critical load (that is, higher than the critical load resistance) results in the inductor current during the off-interval of the transistor to drop to zero, prior to the beginning of the next switching cycle, as shown in Fig. 3A-1a. The inductor current i_L cannot reverse through the diode, and hence becomes discontinuous, remaining zero until the beginning of the new switching cycle. The normalized off interval of the transistor now consists of two subintervals: $D_{off,1}$ and $D_{off,2}$, such that $(D + D_{off,1} + D_{off,2}) = 1$. During $D_{off,2}$, v_A jumps from 0 to V_o as shown in Fig. 3A-1a. The extra volt-seconds, shown as the area hatched in Fig. 3A-1a, averaged over the switching-cycle, result in the output voltage V_o to go higher than its CCM value. The output voltage is plotted in Fig. 3A-1b for a duty-ratio D, which shows that at very light loads in DCM, the output voltage approaches V_{in}. A detailed derivation is presented in the Appendix on the accompanying CD.

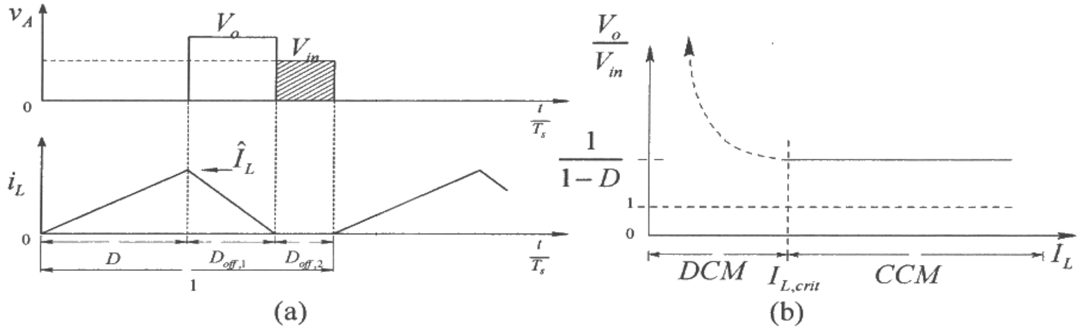


(a) (b)

Figure 3A-1 Buck converter in DCM.

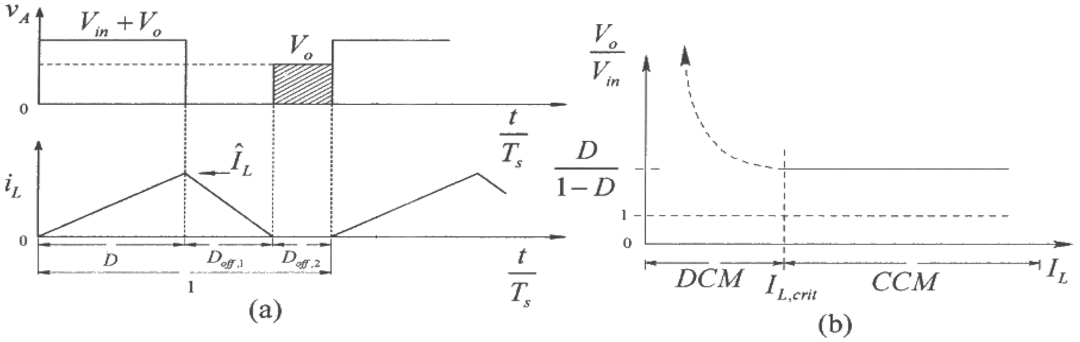
3A-1-2 Boost and Buck-Boost Converters in DCM

Unlike Buck converters, Boost and Buck-Boost converters represent a special challenge in DCM, where at very light loads, their output voltage, if not properly regulated can reach dangerously high values, and therefore, care should be taken to avoid this condition. Only the waveforms and the plot of the voltage conversion ratio are presented here in Fig. 3A-2 and Fig. 3A-3 respectively, and the detailed discussion is included in the accompanying CD.



v_A
V_o
V_{in}
0
$\frac{t}{T_s}$
i_L
$\hat{I}_L$
0
D
$D_{off,1}$
$D_{off,2}$
1
$\frac{t}{T_s}$
(a)
$\frac{V_o}{V_{in}}$
$\frac{1}{1-D}$
1
0
DCM
$I_{L,crit}$
CCM
I_L
(b)

Figure 3A-2 Boost converter in DCM.



v_A
$V_{in}+V_o$
V_o
0
$\frac{t}{T_s}$
i_L
$\hat{I}_L$
0
D
$D_{off,1}$
$D_{off,2}$
1
$\frac{t}{T_s}$
(a)
$\frac{V_o}{V_{in}}$
$\frac{D}{1-D}$
1
0
DCM
$I_{L,crit}$
CCM
I_L
(b)

Figure 3A-3 Buck-Boost converter in DCM.

3A-2 AVERAGE REPRESENTATION OF DC-DC CONVERTERS IN DCM

In the previous discussion, we saw that unlike the CCM where the output voltage was independent of the load and was dictated only by the input voltage V_{in} and the transistor duty-ratio $d(t)$, the output voltage in DCM also depends on the converter parameters and the operating condition. The average representation of a switching power-pole in DCM can be obtained by the voltage and current waveforms associated with the converter. In DCM, since the output voltage at the voltage-port is higher than that in the CCM case, the average model of a switching power-pole in CCM by an ideal transformer is augmented by a dependent voltage-source v_k at the current-port and a dependent current-source i_k at the voltage-port. The values of these dependent sources for the three converters are calculated in the Appendix on the accompanying CD, and the results are presented below.

3A-2-1 v_k and i_k for Buck and Buck-Boost Converters in DCM

The average representation of the switching power-pole in Buck and Buck-Boost converters in DCM is shown in Fig. 3A-4 in terms of the dynamic quantities, where

$$v_{k,Buck} = [1 - \frac{2Lf_s\bar{i}_L}{(V_{in}-\bar{v}_o)d}]\bar{v}_0 \qquad (3A\text{-}1)$$

$$i_{k,Buck} = \frac{d^2}{2Lf_s}(V_{in} - \overline{v}_0) - d\overline{i}_L \tag{3A-2}$$

$$v_{k,Buck-Boost} = \left(1 - \frac{2Lf_s\overline{i}_L}{V_{in}d}\right)\overline{v}_o \tag{3A-3}$$

$$i_{k,Buck-Boost} = \frac{d^2}{2Lf_s}V_{in} - d\overline{i}_L \tag{3A-4}$$

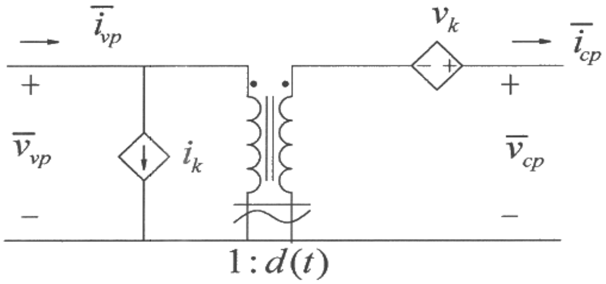


Figure 3A-4 Average dynamic model for Buck and Buck-Boost converters.

If v_k and i_k are conditional such that they are both zero in CCM and are expressed by the above expressions only in DCM where the average inductor current falls below the critical value, then the representation in Fig. 3A-4 becomes valid for both the CCM and the DCM.

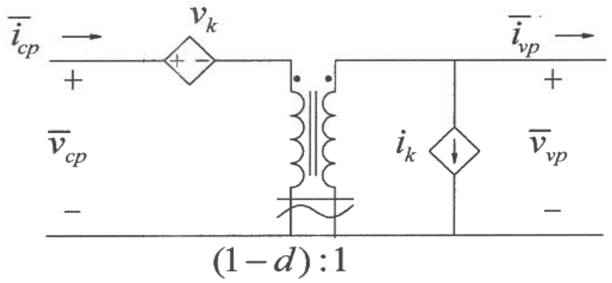
In PSpice the ideal transformer itself is represented by a dependent current source and a dependent voltage sources. The conditional dependent sources v_k and i_k shown in Fig. 3A-4 are in addition to those used to represent the ideal transformer.

3A-2-2 v_k and i_k for Boost Converters in DCM

The average representation of the switching power-pole in Boost converters in DCM is shown in Fig. 3A-5 in terms of the dynamic quantities, where

$$v_{k,Boost} = \left(1 - \frac{2Lf_s\overline{i}_L}{V_{in}d}\right)(V_{in} - \overline{v}_0) \tag{3A-5}$$

$$i_{k,Boost} = \frac{d^2}{2Lf_s}V_{in} - d\overline{i}_L \tag{3A-6}$$



$\overline{i}_{cp}$
v_k
$\overline{i}_{vp}$
+
$\overline{v}_{cp}$
−
i_k
+
$\overline{v}_{vp}$
−
$(1-d):1$

Figure 3A-5 Average dynamic model for Boost converters.

By expressing v_k and i_k conditionally such that they are both zero in CCM and are expressed by Eqs. 3A-5 and 3A-6 only in DCM where the average inductor current falls below the critical value, the representation in Fig. 3A-5 becomes valid for both the CCM and the DCM.

Chapter 4

DESIGNING FEEDBACK CONTROLLERS IN SWITCH-MODE DC POWER SUPPLIES

4-1 INTRODUCTION AND OBJECTIVES OF FEEDBACK CONTROL

As shown in Fig. 4-1, almost all dc-dc converters operate with their output voltage regulated to equal their reference value within a specified tolerance band (for example, ± 1 % around its nominal value) in response to disturbances in the input voltage and the output load. This regulation is achieved by pulsed-width-modulating the duty-ratio $d(t)$ of their switching power-pole. In this chapter, we will design the feedback controller to regulate the output voltages of dc-dc converters.

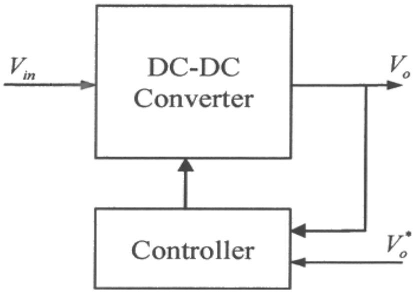


Figure 4-1 Regulated dc power supply.

The feedback controller to regulate the output voltage must be designed with the following objectives in mind: zero steady state error, fast response to changes in the input voltage and the output load, low overshoot, and low noise susceptibility. We should note that in designing feedback controllers, all transformer-isolated topologies discussed later in Chapter 8 can be replaced by their basic single-switch topologies from which they are derived. The feedback control is described using the voltage-mode control, which is later extended to include the current-mode control.

The steps in designing the feedback controller are described as follows:

- Linearize the system for small changes around the dc steady state operating point (bias point). This requires dynamic averaging discussed in the previous chapter.
- Design the feedback controller using linear control theory.

- Confirm and evaluate the system response by simulations for large disturbances.

4-2 REVIEW OF LINEAR CONTROL THEORY

A feedback control system is as shown in Fig. 4-2, where the output voltage is measured and compared with a reference value V_o^*. The error between the two acts on the controller, which produces the control voltage $v_c(t)$. This control voltage acts as the input to the pulse-width-modulator to produce a switching signal $q(t)$ for the power-pole in the dc-dc converter. The average value of this switching signal is $d(t)$, as shown in Fig. 4-2.

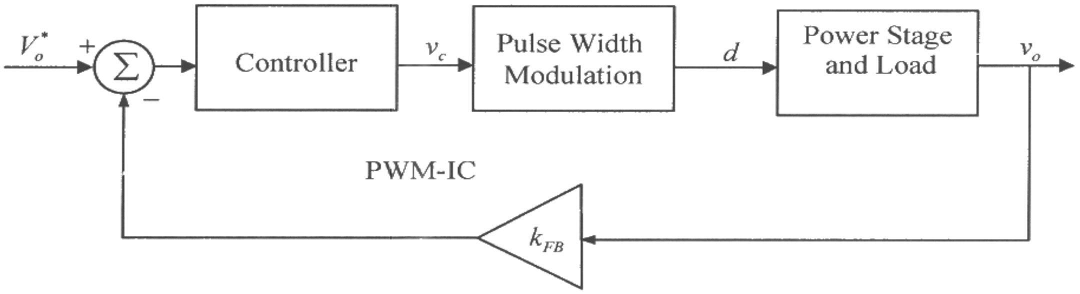


Figure 4-2 Feedback control.

To make use of linear control theory, various blocks in the power supply system of Fig. 4-2 are linearized around the steady state dc operating point, assuming small-signal perturbations. Each average quantity (represented by a "-" on top) associated with the power-pole of the converter topology can be expressed as the sum of its steady state dc value (represented by an uppercase letter) and a small-signal perturbation (represented by a "~" on top), for example,

$$\begin{aligned} \bar{v}_o(t) &= V_o + \tilde{v}_o(t) \\ d(t) &= D + \tilde{d}(t) \\ v_c(t) &= V_c + \tilde{v}_c(t) \end{aligned} \qquad (4\text{-}1)$$

where $d(t)$ is already an averaged value and $v_c(t)$ does not contain any switching frequency component. Based on the small-signal perturbation quantities in the Laplace domain, the linearized system block diagram is as shown in Fig. 4-3, where the perturbation in the reference input to this feedback-controlled system, $\tilde{v}_o^*$, is zero since the output voltage is being regulated to its reference value. In Fig. 4-3, $G_{PWM}(s)$ is the transfer function of the pulse-width modulator, and $G_{PS}(s)$ is the power stage transfer function. In the feedback path, the transfer function is of the voltage-sensing network, which can be represented by a simple gain k_{FB}, usually less than unity. $G_C(s)$ is the transfer function of the feedback controller that needs to be determined to satisfy the control objectives.

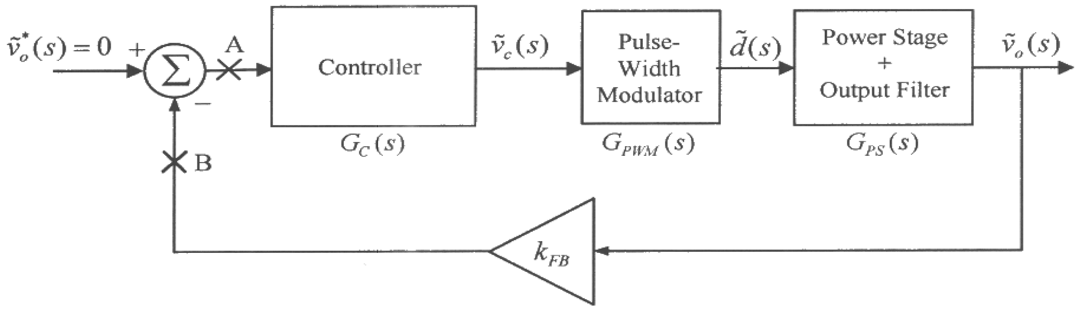


Figure 4-3 Small signal control system representation.

4-2-1 Loop Transfer Function $G_L(s)$

It is the closed-loop response (with the feedback in place) that we need to optimize. Using linear control theory, we can achieve this objective by ensuring certain characteristics of the loop transfer function $G_L(s)$. In the control block diagram of Fig. 4-3, the loop transfer function (from point A to point B) is

$$G_L(s)=G_C(s)G_{PWM}(s)G_{PS}(s)k_{FB} \tag{4-2}$$

4-2-2 Crossover Frequency f_c of $G_L(s)$

In order to define a few necessary control terms, we will consider a generic Bode plot of the loop transfer function $G_L(s)$ in terms of its magnitude and phase angle, shown in Fig. 4-4 as a function of frequency. The frequency at which the gain equals unity (that is $|G_L(s)|=0\,dB$) is defined as the crossover frequency f_c (or ω_c). This crossover frequency is a good indicator of the bandwidth of the closed-loop feedback system, which determines the speed of the dynamic response of the control system to various disturbances.

4-2-3 Phase and Gain Margins

For the closed-loop feedback system to be stable, at the crossover frequency f_c, the phase delay introduced by the loop transfer function must be less than 180^0. At f_c, the phase angle $\angle G_L(s)|_{f_c}$ of the loop transfer function $G_L(s)$, measured with respect to -180^0, is defined as the Phase Margin (ϕ_{PM}) as shown in Fig. 4-4:

$$\phi_{PM}=\angle G_L(s)|_{f_c}-(-180^0)=\angle G_L(s)|_{f_c}+180^0 \tag{4-3}$$

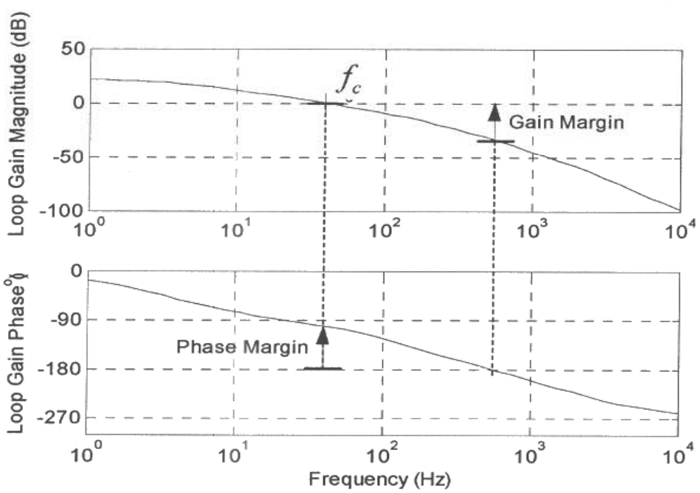


Figure 4-4 Definitions of crossover frequency, gain margin and phase margin.

Note that $\angle G_L(s)|_{f_c}$ is negative, but the phase margin in Eq. 4-3 must be positive. Generally, feedback controllers are designed to yield a phase margin of approximately 60^0, since much smaller values result in high overshoots and long settling times (oscillatory response) and much larger values in a sluggish response.

The Gain Margin is also defined in Fig. 4-4, which shows that the gain margin is the value of the magnitude of the loop transfer function, measured below 0 *dB*, at the frequency at which the phase angle of the loop transfer function may (not always) cross -180^0. If the phase angle crosses -180^0, the gain margin should generally be in excess of 10 *dB* in order to keep the system response from becoming oscillatory due to parameter changes and other variations.

4-3 LINEARIZATION OF VARIOUS TRANSFER FUNCTION BLOCKS

To be able to apply linear control theory in the feedback controller design, it is necessary that all the blocks in Fig. 4-2 be linearized around their dc steady state operating point, as shown by transfer functions in Fig. 4-3.

4-3-1 Linearizing the Pulse-Width Modulator

In the feedback control, a high-speed PWM integrated circuit such as the UC3824 [1] from Unitrode/Texas Instruments may be used. Functionally, within this PWM-IC shown in Fig. 4-5a, the control voltage $v_c(t)$ generated by the error amplifier is compared with a ramp signal v_r with a constant amplitude $\hat{V}_r$ at a constant switching frequency f_s, as shown in Fig. 4-5b. The output switching signal is represented by the switching function $q(t)$, which equals 1 if $v_c(t) \geq v_r$; otherwise 0. The switch duty-ratio in Fig. 4-5b is given as

$$d(t)=\frac{v_c(t)}{\hat{V}_r} \tag{4-4}$$

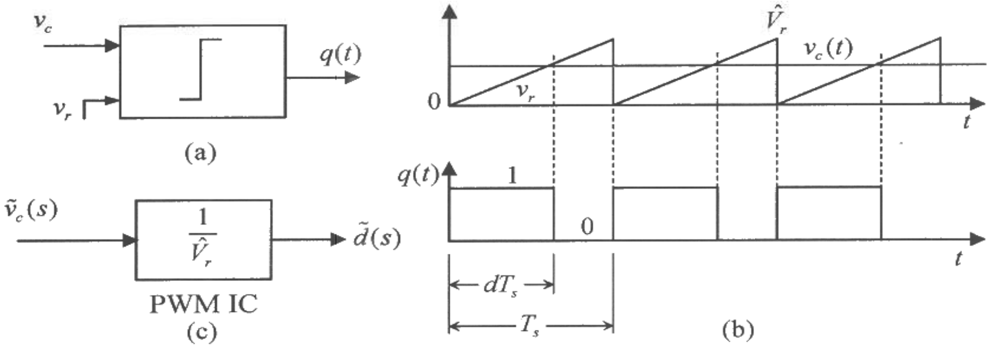


Figure 4-5 PWM waveforms.

In terms of a disturbance around the dc steady state operating point, the control voltage can be expressed as

$$v_c(t)=V_c+\tilde{v}_c(t) \tag{4-5}$$

Substituting Eq. 4-5 into Eq. 4-4,

$$d(t)=\underbrace{\frac{V_c(t)}{\hat{V}_r}}_{D}+\underbrace{\frac{\tilde{v}_c(t)}{\hat{V}_r}}_{\tilde{d}(t)} \tag{4-6}$$

In Eq. 4-6, the second term on the right side equals $\tilde{d}(t)$, from which the transfer function of the PWM-IC is

$$G_{PWM}(s)=\frac{\tilde{d}(s)}{\tilde{v}_c(s)}=\frac{1}{\hat{V}_r} \tag{4-7}$$

It is a constant gain transfer function, as shown in Fig. 4-5c in the Laplace domain.

▲ **Example 4-1** In PWM-ICs, there is usually a dc voltage offset in the ramp voltage, and instead of $\hat{V}_r$ as shown in Fig. 4-5b, a typical Valley-to-Peak value of the ramp signal is defined. In the PWM-IC UC3824, this valley-to-peak value is 1.8 V. Calculate the linearized transfer function associated with this PWM-IC.

Solution The dc offset in the ramp signal does not change its small signal transfer function. Hence, the peak-to-valley voltage can be treated as $\hat{V}_r$. Using Eq. 4-7

$$G_{PWM}(s)=\frac{1}{\hat{V}_r}=\frac{1}{1.8}=0.556 \tag{4-8}$$

▲

4-3-2 Linearizing the Power Stage of DC-DC Converters in CCM

To design feedback controllers, the power stage of the converters must be linearized around the steady state dc operating point, assuming a small-signal disturbance. Fig. 4-6a shows the average model of the switching power-pole, where the subscript "*vp*" refers to the voltage-port and "*cp*" to the current-port. Each average quantity in Fig. 4-6a can be expressed as the sum of its steady state dc value (represented by an uppercase letter) and a small-signal perturbation (represented by a "~" on top):

$$
\begin{aligned}
d(t) &= D + \tilde{d}(t) \\
\bar{v}_{vp}(t) &= V_{vp} + \tilde{v}_{vp}(t) \\
\bar{v}_{cp}(t) &= V_{cp} + \tilde{v}_{cp}(t) \\
\bar{i}_{vp}(t) &= I_{vp} + \tilde{i}_{vp}(t) \\
\bar{i}_{cp}(t) &= I_{cp} + \tilde{i}_{cp}(t)
\end{aligned}
\qquad (4\text{-}9)
$$

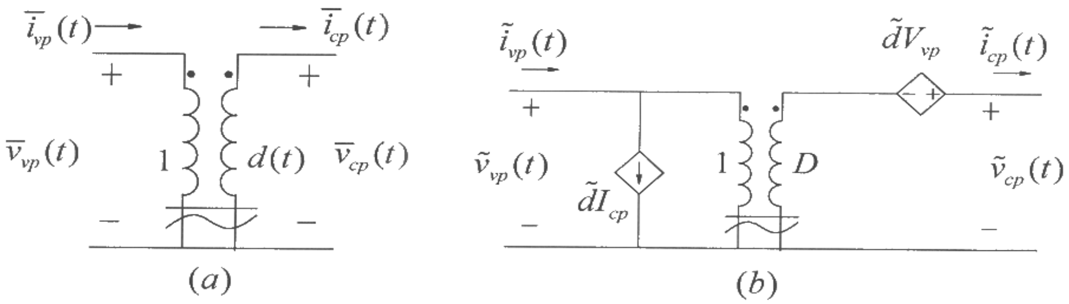


Figure 4-6 Linearizing the switching power-pole.

Utilizing the voltage and current relationships between the two ports in Fig. 4-6a, and expressing each variable as in Eq. 4-9

$$V_{cp} + \tilde{v}_{cp} = (D + \tilde{d})\,(V_{vp} + \tilde{v}_{vp}) \qquad (4\text{-}10a)$$

and,

$$I_{vp} + \tilde{i}_{vp} = (D + \tilde{d})(I_{cp} + \tilde{i}_{cp}) \qquad (4\text{-}10b)$$

Equating the perturbation terms on both sides of the above equations

$$\tilde{v}_{cp}(t) = V_{vp}\tilde{d} + D\tilde{v}_{vp} + \cancel{\tilde{d}\tilde{v}_{vp}} \qquad (4\text{-}11a)$$

and,

$$\tilde{i}_{vp} = D\tilde{i}_{cp} + I_{cp}\tilde{d} + \cancel{\tilde{d}\tilde{i}_{cp}} \qquad (4\text{-}11b)$$

The two equations above are linearized by neglecting the products of small perturbation terms (crossed out in Eqs. 4-11a and b). The resulting linear equations are

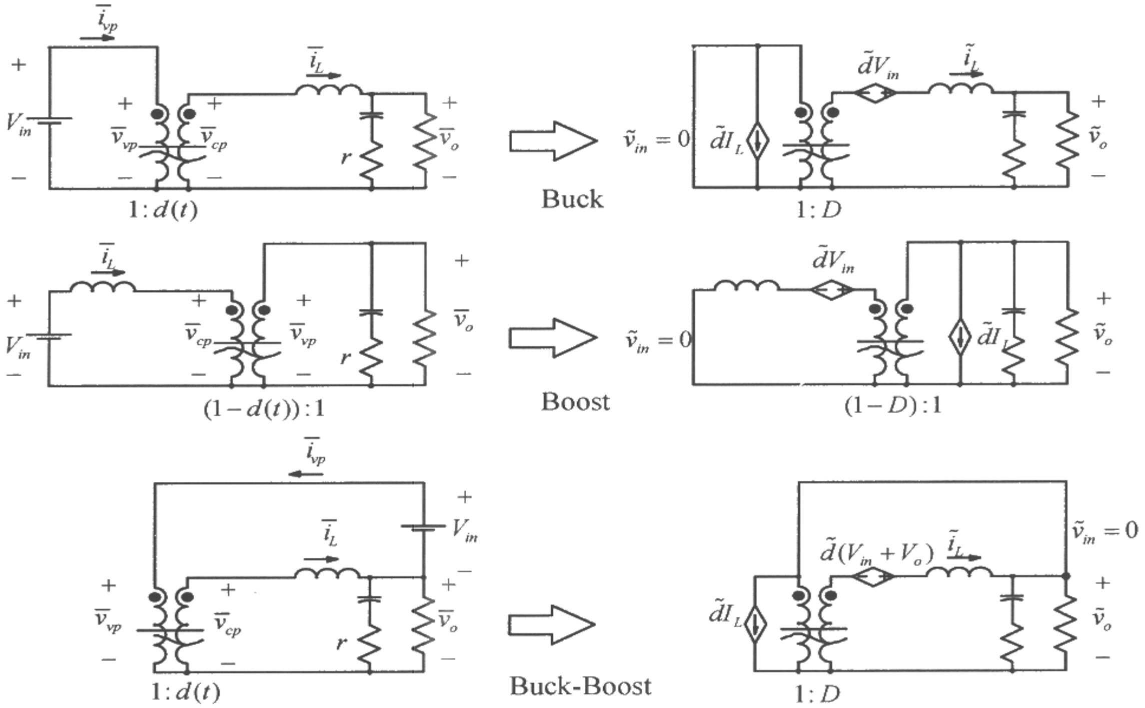
$$\tilde{v}_{cp}(t) = V_{vp}\tilde{d} + D\tilde{v}_{vp} \tag{4-12}$$

and,

$$\tilde{i}_{vp} = D\tilde{i}_{cp} + I_{cp}\tilde{d} \tag{4-13}$$

Eqs. 4-12 and 4-13 can be represented by means of an ideal transformer shown in Fig. 4-6b, which is a linear representation of the power-pole for small signals around a steady state operating point given by D, V_{vp}, and I_{cp}.

The average representations of Buck, Boost and Buck-Boost converters are shown in Fig. 4-7a. Replacing the power-pole in each of these converters by its small-signals linearized representation, the resulting circuits are shown in Fig. 4-7b, where the perturbation $\tilde{v}_{in}$ is zero based on the assumption of a constant dc input voltage V_{in}, and the output capacitor ESR is represented by r. Note that in Boost converters, since the transistor is in the bottom position of the switching power-pole, D in Eqs. 4-12 and 4-13 needs to be replaced by $(1-D)$ and $\tilde{d}$ by $(-\tilde{d})$.



$\bar{i}_{vp}$
V_{in}
$\bar{v}_{vp}$
$\bar{v}_{cp}$
$\bar{i}_L$
r
$\bar{v}_o$
$1:d(t)$
Buck
$\tilde{v}_{in}=0$
$\tilde{d}I_L$
$\tilde{d}V_{in}$
$\tilde{i}_L$
$\tilde{v}_o$
$1:D$
$(1-d(t)):1$
Boost
$(1-D):1$
Buck-Boost
$\tilde{d}(V_{in}+V_o)$
(a)
(b)

Figure 4-7 Linearizing single-switch converters in CCM.

As fully explained in the Appendix on the accompanying CD, all three circuits for small-signal perturbations in Fig. 4-7b have the same form as shown in Fig. 4-8. In this equivalent circuit, the effective inductance L_e is the same as the actual inductance L in the Buck converter, since in both states of a Buck converter in CCM, L and C are always connected together. However, in Boost and Buck-Boost converters, these two elements are not always connected, resulting in L_e to be $L/(1-D)^2$ in Fig. 4-8:

$$L_e = L \text{ (Buck)}; \quad L_e = \frac{L}{(1-D)^2} \text{ (Boost and Buck-Boost)} \tag{4-14}$$

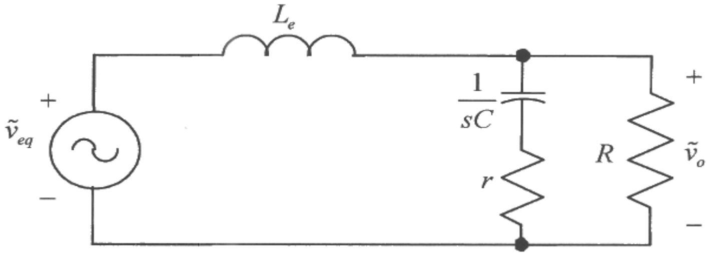


Figure 4-8 Small signal equivalent circuit for Buck, Boost and Buck-Boost converters.

Transfer functions of the three converters in CCM from the Appendix on the accompanying CD are repeated below:

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{V_{in}}{LC} \frac{1+srC}{s^2 + s\left(\frac{1}{RC}+\frac{r}{L}\right)+\frac{1}{LC}} \quad \text{(Buck)} \tag{4-15}$$

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{V_{in}}{(1-D)^2}\left(1-s\frac{L_e}{R}\right) \frac{1+srC}{L_eC\left(s^2 + s\left(\frac{1}{RC}+\frac{r}{L_e}\right)+\frac{1}{L_eC}\right)} \quad \text{(Boost)} \tag{4-16}$$

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{V_{in}}{(1-D)^2}\left(1-s\frac{DL_e}{R}\right) \frac{1+srC}{L_eC\left(s^2 + s\left(\frac{1}{RC}+\frac{r}{L_e}\right)+\frac{1}{L_eC}\right)} \quad \text{(Buck-Boost)} \tag{4-17}$$

In the above power-stage transfer functions in CCM, there are several characteristics worth noting. There are two poles created by the low-pass *L-C* filter in Fig. 4-8, and the capacitor ESR r results in a zero. In Boost and Buck-Boost converters, their transfer functions depend on the steady state operating value D. They also have a right-half-plane zero, whose presence can be explained by the fact that in these converters, increasing the duty-ratio for increasing the output, for example, initially has an opposite consequence by isolating the input stage from the output load for a longer time.

4-3-2-1 Using Computer Simulation to Obtain $\tilde{v}_o/\tilde{d}$

Transfer functions given by Eqs. 4-15 through 4-17 provide theoretical insight into converter operation. However, the Bode plots of the transfer function can be obtained with similar accuracy by means of linearization and ac analysis, using a computer program such as PSpice™. The converter circuit is simulated as shown in Figs. 4-9 in the example below for a frequency-domain ac analysis, using the switching power-pole average model discussed in Chapter 3 and shown in Fig. 4-6a. The duty-cycle perturbation $\tilde{d}$ is represented as an ac source whose frequency is swept over several decades of interest, and whose amplitude is kept constant. In such a simulation, PSpice first calculates voltages and currents at the dc steady state operating point, linearizes the circuit around this dc bias point, and then performs the ac analysis.

▲ **Example 4-2** A Buck converter has the following parameters and is operating in CCM: $L = 100\mu H$, $C = 697\mu F$, $r = 0.1\Omega$, $f_s = 100kHz$, $V_{in} = 30V$, and $P_o = 36W$. The duty-ratio D is adjusted to regulate the output voltage $V_o = 12V$. Obtain both the gain and the phase of the power stage $G_{PS}(s)$ for the frequencies ranging from 1 Hz to 100 kHz.

Solution The PSpice circuit is shown in Fig. 4-9 where the dc voltage source {D}, representing the duty-ratio *D*, establishes the dc operating point. The duty-ratio perturbation $\tilde{d}$ is represented as an ac source whose frequency is swept over several decades of interest, keeping the amplitude constant. (Since the circuit is linearized before the ac analysis, the best choice for the ac source amplitude is 1 *V*.) The switching power-pole is represented by an ideal transformer, which consists of two dependent sources: a dependent current source and a dependent voltage source. The circuit parameters are specified by means of parameter blocks within PSpice.

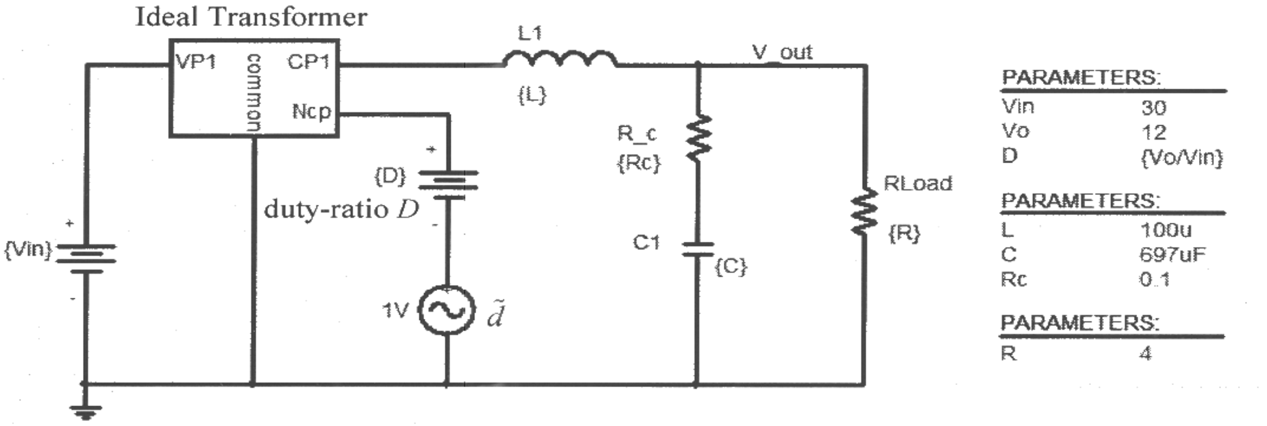


Figure 4-9 PSpice Circuit model for a Buck converter.

The Bode plot of the frequency response is shown in Fig. 4-10. It shows that at the crossover frequency $f_c = 1kHz$ selected in the next example, Example 4-3, the power stage has $\left|G_{PS}(s)\right|_{f_c} = 24.66dB$ and $\angle G_{PS}(s)\Big|_{f_c} = -138^0$. We will make use of these values in Example 4-3.

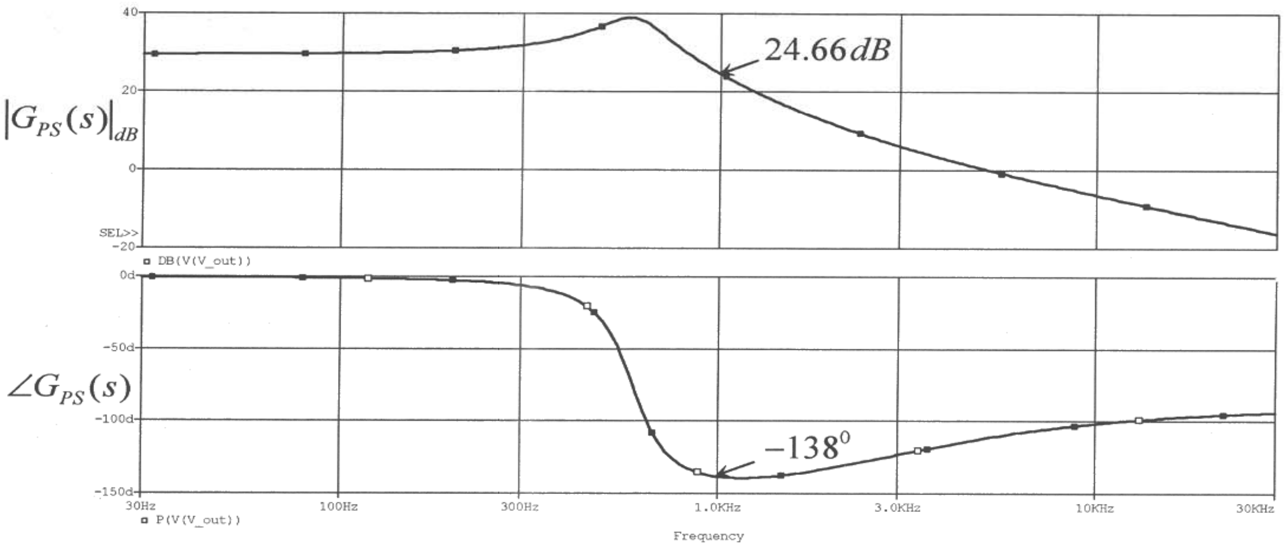


Figure 4-10 The gain and the phase of the power stage $G_{PS}(s)$.

▲

4-4 FEEDBACK CONTROLLER DESIGN IN VOLTAGE-MODE CONTROL

The feedback controller design is presented by means of a numerical example to regulate the Buck converter described in Example 4-2. The controller is designed for the continuous conduction mode (CCM) at full-load, which although not optimum, is stable in DCM.

▲ **Example 4-3** Design the feedback controller for the Buck converter described in Example 4-2. The PWM-IC is as described in Example 4-1. The output voltage-sensing network in the feedback path has a gain $k_{FB} = 0.2$. The steady state error is required to be zero and the phase margin of the loop transfer function should be 60^0 at as high a crossover frequency as possible.

Solution In deciding on the transfer function $G_C(s)$ of the controller, the control objectives translate into the following simultaneous characteristics of the loop transfer function $G_L(s)$, from which $G_C(s)$ can be designed:

1. The crossover frequency f_c of the loop gain is as high as possible to result in a fast response of the closed-loop system.
2. The phase angle of the loop transfer function has the specified phase margin, typically 60^0 at the crossover frequency so that the response in the closed-loop system settles quickly without oscillations.
3. The phase angle of the loop transfer function should not drop below -180^0 at frequencies below the crossover frequency.

The Bode plot for the power stage is obtained earlier, as shown in Fig. 4-10 of Example 4-2. In this Bode plot, the phase angle drops towards -180^0 due to the two poles of the *L-C* filter shown in the equivalent circuit of Fig. 4-8 and confirmed by the transfer function of Eq. 4-15. Beyond the *L-C* filter resonance frequency, the phase angle increases toward -90^0 because of the zero introduced by the output capacitor ESR in the transfer function of the power stage. We should not rely on this capacitor ESR, which is not accurately known and can have a large variability.

A simple procedure based on the K-factor approach [2] is presented below, which lends itself to a straightforward step-by-step design. For reasons given below, the transfer function $G_C(s)$ of the controller is selected to be of the form in Eq. 4-18 whose Bode plot is shown in Fig. 4-11.

$$G_C(s) = \frac{k_c}{s} \underbrace{\frac{(1+s/\omega_z)^2}{(1+s/\omega_p)^2}}_{phase-boost} \qquad (4\text{-}18)$$

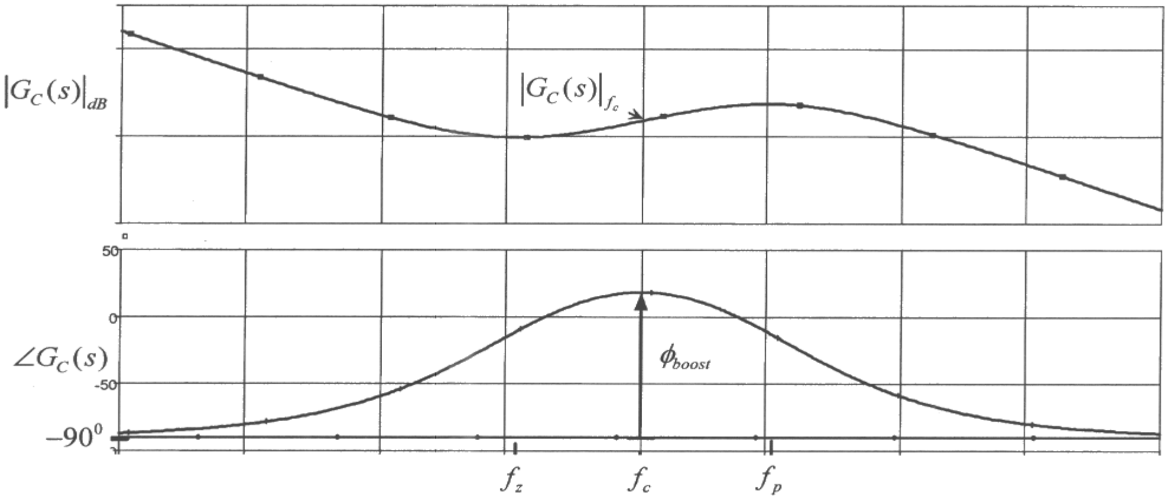


Figure 4-11 Bode plot of $G_C(s)$ in Eq. 4-18.

To yield a zero steady state error, $G_C(s)$ contains a pole at the origin, which introduces -90^0 phase shift in the loop transfer function. The crossover frequency f_c of the loop is chosen beyond the *L-C* resonance frequency of the power stage, where, unfortunately, $\angle G_{PS}|_{f_c}$ has a large negative value. The sum of -90^0, due to the pole at the origin in $G_C(s)$, and $\angle G_{PS}|_{f_c}$ is more negative than -180^0. Therefore, to obtain a phase margin of 60^0 requires boosting the phase at f_c, by more than 90^0, by placing two coincident zeroes at f_z to nullify the effect of the two poles in the power-stage transfer function

$G_{PS}(s)$. Two coincident poles are placed at f_p ($> f_z$) to roll-off the gain rapidly much before the switching frequency. The controller gain $|G_C(s)|_{f_c}$ is such that the loop gain equals unity at the crossover frequency.

The input specifications in determining the parameters of the controller transfer function in Eq. 4-18 are f_c, ϕ_{boost} as shown in Fig. 4-11, and the controller gain $|G_C(s)|_{f_c}$. A step-by-step procedure for designing $G_C(s)$ is described below.

Step 1: Choose the Crossover Frequency. Choose f_c to be *slightly* beyond the *L-C* resonance frequency $1/(2\pi\sqrt{LC})$, which in this example is approximately 600 Hz. Therefore, we will choose $f_c = 1\text{ kHz}$. This ensures that the phase angle of the loop remains greater than -180^0 at all frequencies.

Step 2: Calculate the needed Phase Boost. The desired phase margin is specified as $\phi_{PM} = 60^0$. The required phase boost ϕ_{boost} at the crossover frequency is calculated as follows, noting that G_{PWM} and k_{FB} produce zero phase shift:

$$\angle G_L(s)|_{f_c} = \angle G_{PS}(s)|_{f_c} + \angle G_C(s)|_{f_c} \qquad \text{(from Eq. 4-2)} \qquad (4\text{-}19)$$

$$\angle G_L(s)|_{f_c} = -180^o + \phi_{PM} \qquad \text{(from Eq. 4-3)} \qquad (4\text{-}20)$$

$$\angle G_C(s)|_{f_c} = -90^o + \phi_{boost} \qquad \text{(from Fig. 4-11)} \qquad (4\text{-}21)$$

Substituting Eqs. 4-20 and 4-21 into Eq. 4-19,

$$\phi_{boost} = -90^o + \phi_{PM} - \angle G_{PS}(s)|_{f_c} \qquad (4\text{-}22)$$

In Fig. 4-10, $\angle G_{PS}(s)|_{f_c} \simeq -138^0$, substituting which in Eq. 4-22 yields the required phase boost $\phi_{boost} = 108^o$.

Step 3: Calculate the Controller Gain at the Crossover Frequency. From Eq. 4-2 at the crossover frequency f_c

$$|G_L(s)|_{f_c} = |G_C(s)|_{f_c} \times |G_{PWM}(s)|_{f_c} \times |G_{PS}(s)|_{f_c} \times k_{FB} = 1 \qquad (4\text{-}23)$$

In Fig. 4-10, at $f_c = 1kHz$, $|G_{PS}(s)|_{f_c=1kHz} = 24.66dB = 17.1$. Therefore in Eq. 4-23, using the gain of the PWM block calculated in Example 4-1,

$$|G_C(s)|_{f_c} \times \underbrace{0.556}_{|G_{PWM}(s)|_{f_c}} \times \underbrace{17.1}_{|G_{PS}(s)|_{f_c}} \times \underbrace{0.2}_{k_{FB}} = 1 \qquad (4\text{-}24)$$

or

$$|G_C(s)|_{f_c} = 0.5263 \tag{4-25}$$

The controller in Eq. 4-18 with two pole-zero pairs is thoroughly analyzed in the Appendix to this chapter on the accompanying CD. According to this analysis, the phase angle of $G_C(s)$ in Eq. 4-18 reaches its maximum at the geometric mean frequency $\sqrt{f_z f_p}$, where the phase boost ϕ_{boost}, as shown in Fig. 4-11, is measured with respect to -90^0. By proper choice of the controller parameters, the geometric mean frequency is made equal to the crossover frequency f_c. We introduce a factor K_{boost} that indicates the geometric separation between poles and zeroes to yield the necessary phase boost:

$$K_{boost} = \sqrt{\frac{\omega_p}{\omega_z}} \tag{4-26}$$

As shown in the Appendix, this factor can be derived in terms of ϕ_{boost} as

$$K_{boost} = \tan\left(45^o + \frac{\phi_{boost}}{4}\right), \tag{4-27}$$

In terms of K_{boost}, from Eqs 4-26 and 4-27, the controller parameters can be calculated as follows:

$$f_z = \frac{f_c}{K_{boost}} \tag{4-28}$$

$$f_p = K_{boost} f_c \tag{4-29}$$

$$k_c = |G_C(s)|_{f_c} \frac{\omega_z}{K_{boost}} \tag{4-30}$$

Once the parameters in Eq. 4-18 are determined, the controller transfer function can be synthesized by a single op-amp circuit shown in Fig. 4-12.

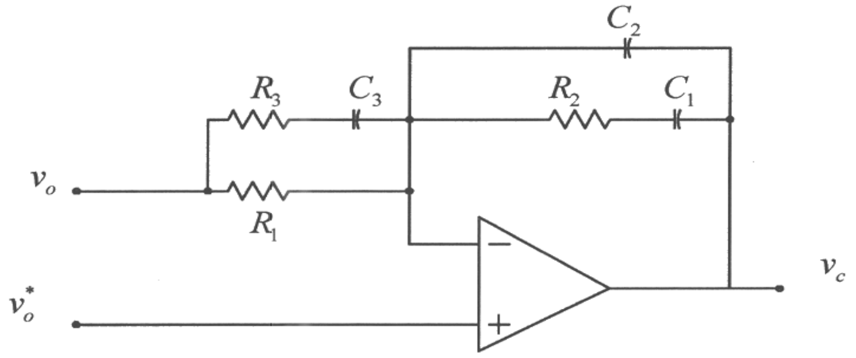


Figure 4-12 Implementation of the controller in Eq. 4-18 by an op-amp.

The choice of R_1 in Fig. 4-12 is based on how much current can be drawn from the sensor output; other resistances and capacitances are chosen using the relationships derived in the Appendix and presented below:

$$\begin{aligned} C_2 &= \omega_z/(k_c\omega_p R_1) \\ C_1 &= C_2\left(\omega_p/\omega_z - 1\right) \\ R_2 &= 1/(\omega_z C_1) \\ R_3 &= R_1/(\omega_p/\omega_z - 1) \\ C_3 &= 1/(\omega_p R_3) \end{aligned} \tag{4-31}$$

In this numerical example with $f_c = 1$ kHz, $\phi_{boost} = 108^o$, and $|G_C(s)|_{f_c} = 0.5263$, we can calculate $K_{boost} = 3.078$ in Eq. 4-27. Using Eqs. 4-27 through 4-30, $f_z = 324.9\,Hz$, $f_p = 3078\,Hz$, and $k_c = 349.1$. For the op-amp implementation, we will select $R_1 = 100\,k\Omega$. From Eq. 4-30, $C_2 = 3.0\,nF$, $C_1 = 25.6\,nF$, $R_2 = 19.1\,k\Omega$, $R_3 = 11.8\,k\Omega$, and $C_3 = 4.4\,nF$. We can verify the design of Example 4-3 in PSpice by adding the controller to the converter model. Notice that the op amp is modeled as a high-gain differential amplifier in Fig. 4-13, where a step-change in load is applied at 1 ms. The results are plotted in Fig. 4-14.

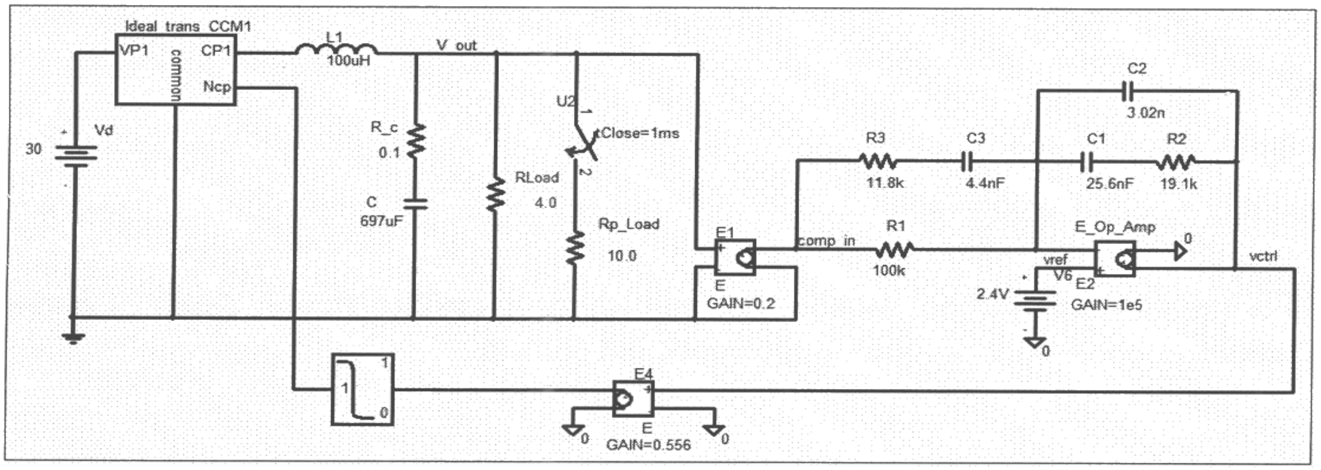

Ideal_trans_CCM1
VP1
common
CP1
Ncp
L1
100uH
V_out
30
Vd
R_c
0.1
C
697uF
RLoad
4.0
U2
1
2
tClose=1ms
Rp_Load
10.0
E1
E
GAIN=0.2
comp_in
R3
11.8k
C3
4.4nF
C2
3.02n
C1
25.6nF
R2
19.1k
R1
100k
E_Op_Amp
0
vref
V6
E2
2.4V
GAIN=1e5
0
vctrl
1
1
0
E4
E
GAIN=0.556
0
0

Figure 4-13 PSpice average model of the Buck converter with voltage-mode control.

Note that in the controller transfer function $G_C(s)$ in the example above, both zeroes are at the same frequency; the same is true for both the poles. This need not be the case for possibly achieving a higher crossover frequency.

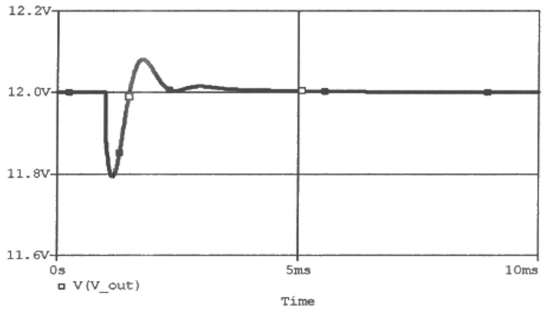


Figure 4-14 Response to a step-change in load.

4-5 PEAK-CURRENT MODE CONTROL

Current-mode control is often used in practice due to its many desirable features, such as simpler controller design and inherent current limiting. In such a control scheme, an inner control loop inside the outer voltage-loop is used as shown in Fig. 4-15, resulting in a peak-current-mode control system. In this control arrangement, another state-variable, the inductor current, is utilized as a feedback signal.

The overall voltage-loop objectives in the current-mode control are the same as in the voltage-mode control discussed earlier. However, the voltage-loop controller here produces the reference value for the current that should flow through the inductor, hence the name current-mode control. There are two types of current-mode control:

- Peak-Current-Mode Control, and
- Average-Current-Mode Control.

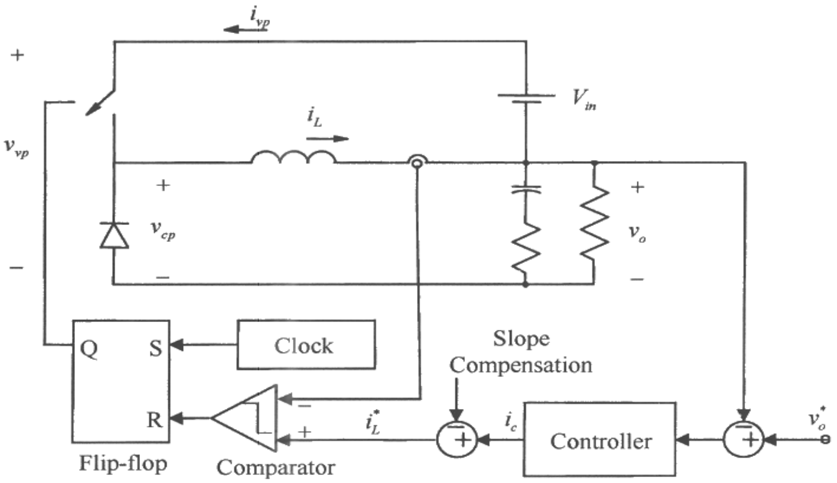


Figure 4-15 Peak current mode control.

In switch-mode dc power supplies, peak-current-mode control is invariably used, and therefore we will concentrate on it here. (We will examine the average-current-mode control in connection with the power-factor-correction circuits discussed in the next chapter.)

For the current loop, the outer voltage loop in Fig. 4-15 produces the reference value i_L^* of the inductor current. This reference current signal is compared with the measured inductor current i_L to reset the flip-flop when i_L reaches i_L^*. As shown in Figs. 4-15 and 4-16a, in generating i_L^*, the voltage controller output i_c is modified by a signal called the slope compensation, which is necessary to avoid oscillations at the sub-harmonic frequencies of f_s, particularly at the duty-ratio $d > 0.5$. Generally, the slope of this compensation signal is less than one-half of the slope at which the inductor current falls when the transistor in the converter is turned off.

In Fig. 4-16a, when the inductor current reaches the reference value, the transistor is turned off, and is turned back on at a regular interval $T_s (= 1/f_s)$ set by the clock. For small perturbations, this current loop acts extremely fast, and it can be assumed ideal with a gain of unity in the small-signal block diagram of Fig. 4-16b. The design of the outer voltage loop is described by means of the example below of a Buck-Boost converter operating in CCM.

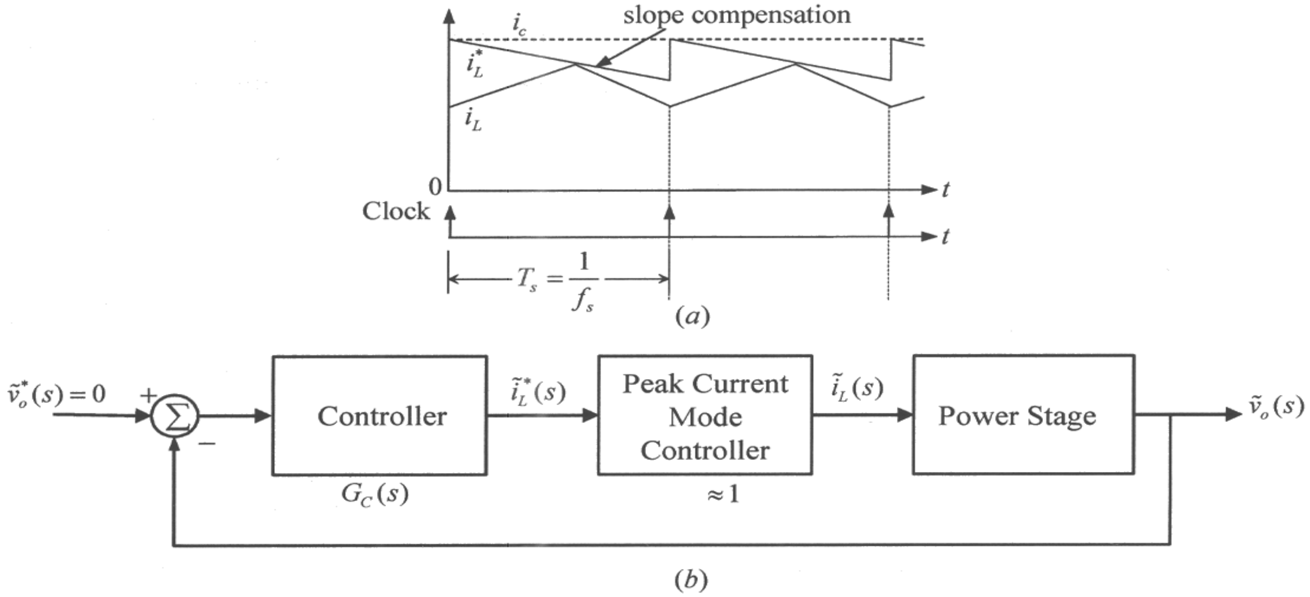


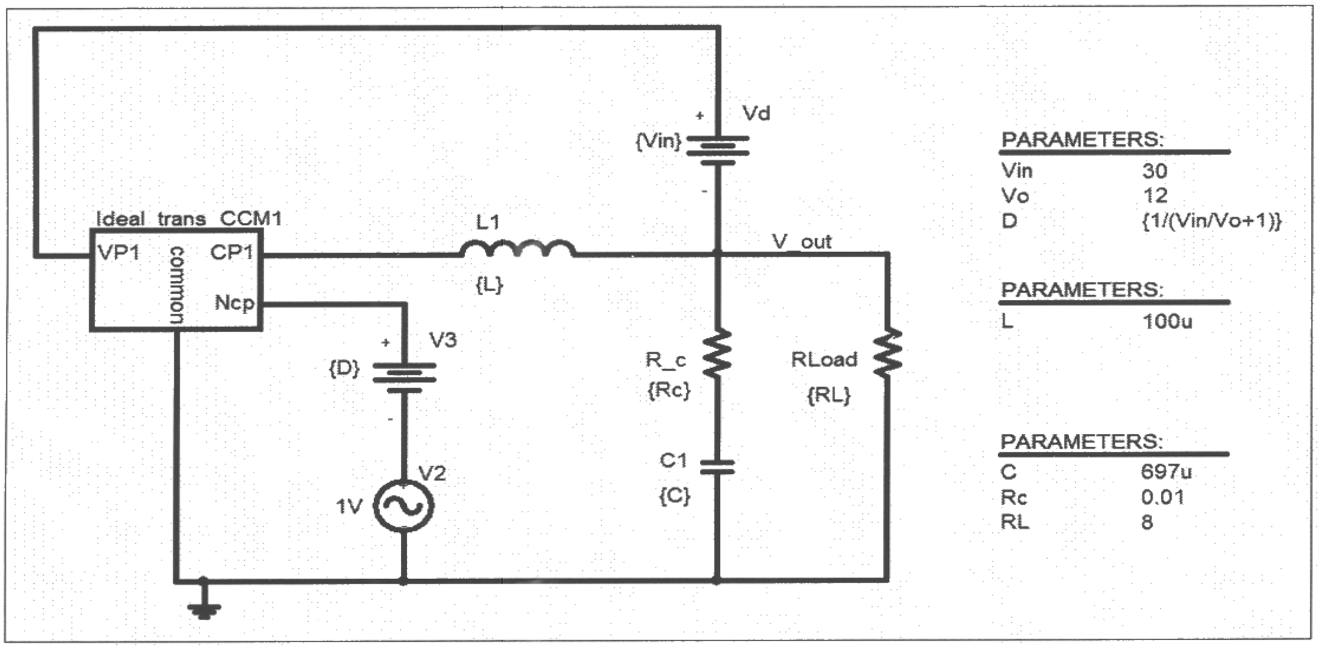
Figure 4-16 Peak-current-mode control with slope compensation.

▲ **Example 4-4** In this example, we will design a peak-current-mode controller for a Buck-Boost converter that has the following parameters and operating conditions: $L = 100\,\mu\text{H}$, $C = 697\,\mu\text{F}$, $r = 0.01\,\Omega$, $f_s = 100\text{ kHz}$, $V_{in} = 30\,\text{V}$. The output power $P_o = 18\,\text{W}$ in CCM and the duty-ratio D is adjusted to regulate the output voltage

$V_o = 12\,\text{V}$. The phase margin required for the voltage loop is 60^0. Assume that in the voltage feedback network, $k_{FB} = 1$.

Solution In designing the outer voltage loop in Fig. 4-16b, the transfer function needed for the power stage is $\tilde{v}_o / \tilde{i}_L$. This transfer function in CCM can be obtained theoretically. However, it is much easier to obtain the Bode plot of this transfer function by means of a computer simulation, similar to that used for obtaining the Bode plots of $\tilde{v}_o / \tilde{d}$ in Example 4-2 for a Buck converter. The PSpice simulation diagram is shown in Fig. 4-17 for the Buck-Boost converter, where, as discussed earlier, an ideal transformer is used for the average representation of the switching power-pole in CCM.

In Fig. 4-17, the dc voltage source represents the switch duty-ratio D and establishes the dc steady state, around which the circuit is linearized. In the ac analysis, the frequency of the ac source, which represents the duty-ratio perturbation $\tilde{d}$, is swept over the desired range, and the ratio of $\tilde{v}_o(s)$ and $\tilde{i}_L(s)$ yields the Bode plot of the power stage $G_{PS}(s)$, as shown in Fig. 4-18.



Vd
{Vin}
+
-
Ideal_trans_CCM1
VP1
common
CP1
Ncp
L1
{L}
V_out
+
V3
{D}
-
V2
1V
R_c
{Rc}
C1
{C}
RLoad
{RL}
PARAMETERS:
Vin 30
Vo 12
D {1/(Vin/Vo+1)}
PARAMETERS:
L 100u
PARAMETERS:
C 697u
Rc 0.01
RL 8

Figure 4-17 PSpice circuit for the Buck-Boost converter.

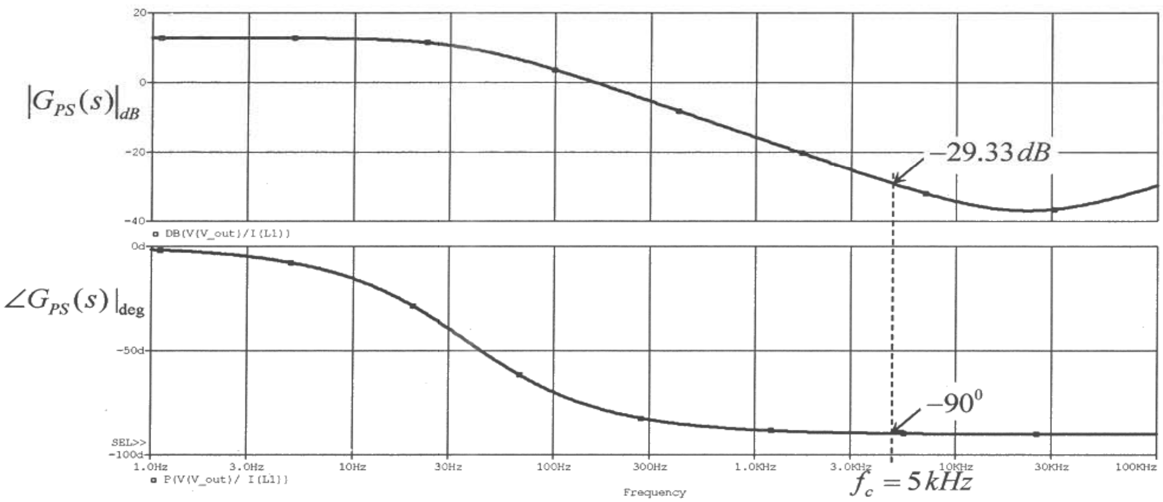


Figure 4-18 Bode plot of $\tilde{v}_o / \tilde{i}_L$.

As shown in Fig. 4-18, the phase angle of the power-stage transfer function levels off at approximately -90^0 at $\sim 1kHz$. The crossover frequency is chosen to be $f_c = 5kHz$, at which in Fig. 4-18, $\angle G_{PS}(s)\big|_{f_c} \simeq -90^0$. As explained in the Appendix on the accompanying CD, the power-stage transfer function $\tilde{v}_o(s)/\tilde{i}_L(s)$ of Buck-Boost converters contains a right-half-plane zero in CCM. The crossover frequency is chosen well below the frequency of the right-half-plane zero for reasons discussed in the Appendix.

To achieve the desired phase margin of 60^0, the controller transfer function is chosen as expressed as below:

$$G_C(s) = \frac{k_c}{s} \underbrace{\frac{(1 + s/\omega_z)}{(1 + s/\omega_p)}}_{phase-boost} \tag{4-32}$$

To yield zero steady state error, it contains a pole at the origin which introduces a -90^0 phase angle. The phase-boost required from this pole-zero combination in Eq. 4-32, using Eq. 4-22 and $\angle G_{PS}(s)\big|_{f_c} \simeq -90^0$, is $\phi_{boost} \simeq 60^0$. Therefore, unlike the controller transfer function of Eq. 4-18 for the voltage-mode control, only a single pole-zero pair is needed to provide phase boost. In Eq. 4-32, the zero and pole frequencies associated with the required phase boost can be derived, as shown in the Appendix on the accompanying CD, where K_{boost} is defined the same as in Eq. 4-26:

$$K_{boost} = \tan\left(45^o + \frac{\phi_{boost}}{2}\right) \tag{4-33}$$

$$f_z = \frac{f_c}{K_{boost}} \tag{4-34}$$

$$f_p = K_{boost} f_c \tag{4-35}$$

$$k_c = \omega_z \left|G_C(s)\right|_{f_c} \tag{4-36}$$

At the crossover frequency, as shown in Fig. 4-18, the power stage transfer function has a gain $\left|G_{PS}(s)\right|_{f_c} = -29.33\,dB$. Therefore, at the crossover frequency, by definition, in Fig. 4-16b

$$\left|G_C(s)\right|_{f_c} \times \left|G_{PS}(s)\right|_{f_c} = 1 \tag{4-37}$$

Hence,

$$\left|G_C(s)\right|_{f_c} = 29.33\,dB = 29.27 \tag{4-38}$$

Using the equations above for $f_c = 5\,kHz$, $\phi_{boost} \simeq 60^0$, and $\left|G_C(s)\right|_{f_c} = 29.27$, $K_{boost} = 3.732$ in Eq. 4-32. Therefore, the parameters in the controller transfer function of Eq. 4-31 are calculated as $f_z = 1340\,Hz$, $f_p = 18660\,Hz$, and $k_c = 246.4 \times 10^3$.

The transfer function of Eq. 4-32 can be realized by an op-amp circuit shown in Fig. 4-19. In the expressions derived in the Appendix, selecting $R_1 = 10\,k\Omega$ and using the transfer-function parameters calculated above, the component values in the circuit of Fig. 4-19 are as follows:

$$\begin{aligned} C_2 &= \frac{\omega_z}{\omega_p R_1 k_c} = 30\ p\text{F} \\ C_1 &= C_2\left(\omega_p / \omega_z - 1\right) = 380\,p\text{F} \\ R_2 &= 1/(\omega_z C_1) = 315\,k\Omega \end{aligned} \tag{4-39}$$

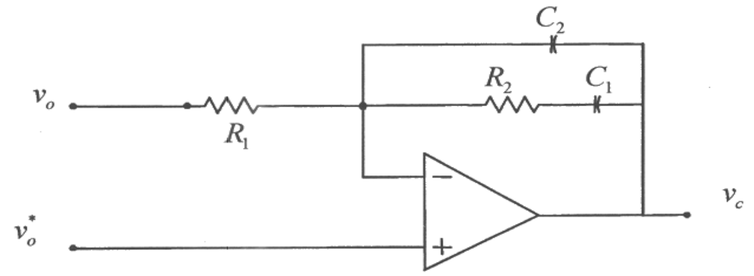


Figure 4-19 Implementation of controller in Eq. 4-32 by an op-amp circuit.

The PSpice circuit diagram is shown in Fig. 4-20 where a load change occurs at 3 ms. Using this simulation, the output voltage and its average are plotted in Fig. 4-21.

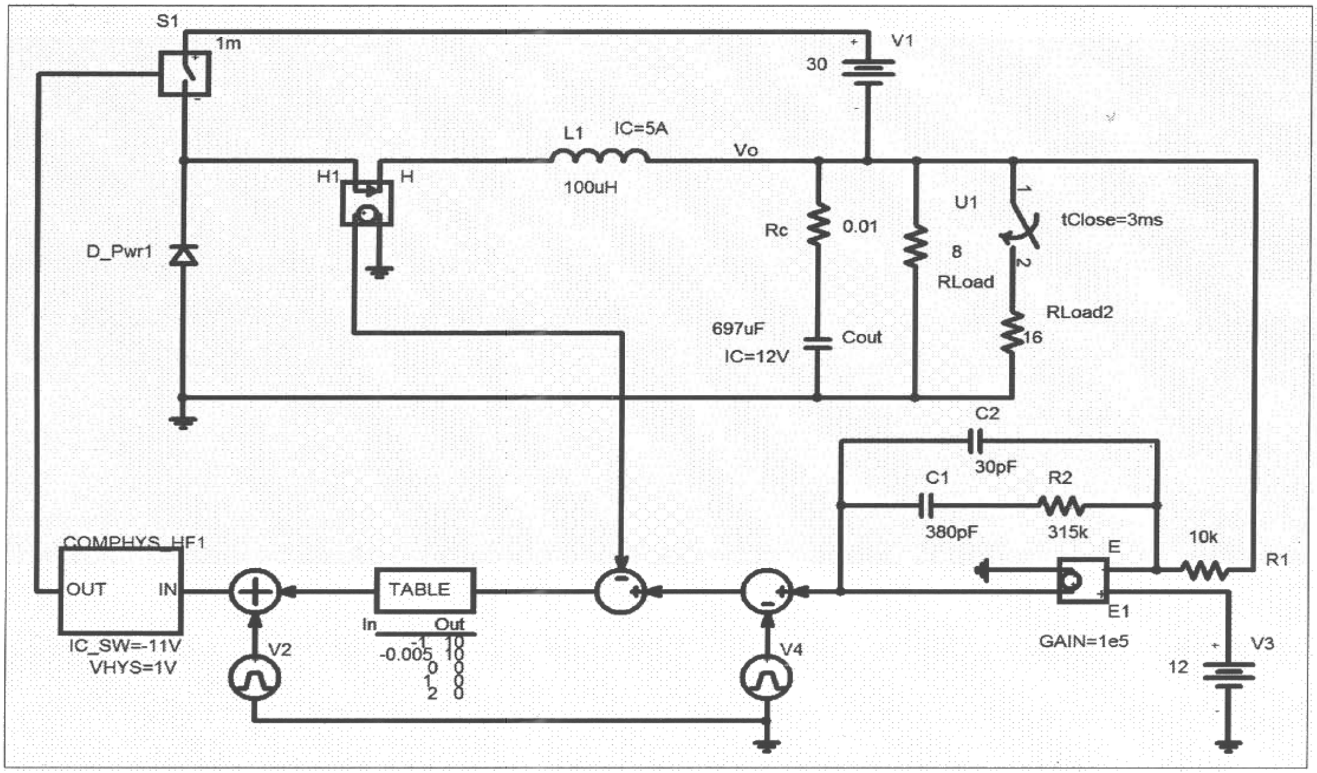

S1
1m
V1
30
L1
IC=5A
100uH
Vo
H1
H
D_Pwr1
Rc
0.01
U1
tClose=3ms
8
RLoad
RLoad2
16
697uF
IC=12V
Cout
C2
30pF
C1
380pF
R2
315k
10k
R1
E
E1
GAIN=1e5
COMPHYS_HF1
OUT
IN
IC_SW=-11V
VHYS=1V
V2
TABLE
In
Out
-1 10
-0.005 10
0 0
1 0
2 0
V4
V3
12

Figure 4-20 PSpice simulation diagram of the peak-current-mode control.

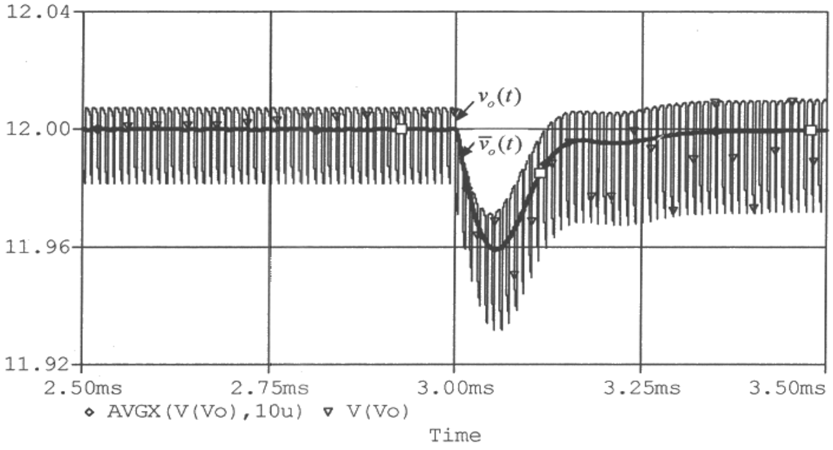


Figure 4-21 Peak current mode control: Output voltage waveform.

▲

4-6 FEEDBACK CONTROLLER DESIGN IN DCM

In sections 4-4 and 4-5, feedback controllers were designed for CCM operation of the converters. The procedure for designing controllers in DCM is the same, except the average model of the power stage in PSpice simulations can be simply replaced by its model which is also valid in DCM, as described in Chapter 3.

REFERENCES

1. Unitrode PWM IC (www.unitrode.com)
2. H. Dean Venable, "The K-Factor: A New Mathematical Tool for Stability Analysis and Synthesis," Proceedings of Powercon 10 (http://www.venable.biz).
3. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.

PROBLEMS

4-1 In a voltage mode controlled DC-DC converter the loop transfer function has the crossover frequency $f_c = 2\,kHz$. The power stage transfer function has a phase angle of -160^0 at the crossover frequency. Calculate w_z and w_p in the voltage controller transfer function of Eq. 4-18, if the required phase margin is 60^0.

4-2 In the above problem the power stage has a gain equal to 20 at the crossover frequency, $k_{FB} = 0.2$, and $G_{PWM} = 0.6$. Calculate k_c in the voltage controller transfer function of Eq. 4-18.

4-3 In a peak-current-mode controlled DC-DC converter the loop crossover frequency in the outer voltage loop is 10 *kHz*. At this crossover frequency, the power stage in Fig. 4-16b has the gain of 0.1, and the phase angle of -80^0. Calculate f_z and f_p in the controller transfer function of Eq. 4-32 if the desired phase margin is 60^0.

Chapter 5

RECTIFICATION OF UTILITY INPUT USING DIODE RECTIFIERS

5-1 INTRODUCTION

Power electronic systems generally get their power from the utility source, as shown by the block diagram in Fig. 5-1. Unless a corrective action is taken as described in the next chapter, this power is drawn by means of highly distorted currents, which have a deleterious effect on the power quality of the utility source. Furthermore, the power system disturbances in the utility source can disrupt the power electronics system's operation. Both of these issues are examined in this chapter.

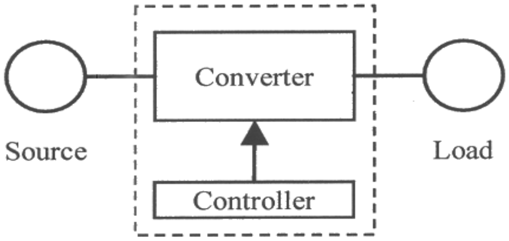


Figure 5-1 Block diagram of power electronic systems.

5-2 DISTORTION AND POWER FACTOR

To quantify distortion in the current drawn by power electronic systems, it is necessary to define certain indices. As a base case, consider the linear $R-L$ load shown in Fig. 5-2a which is supplied by a sinusoidal source in steady state. The voltage and current phasors are shown in Fig. 5-2b, where ϕ is the angle by which the current lags the voltage. Using rms values for the voltage and current magnitudes, the average power supplied by the source is

$$P = V_s I_s \cos\phi \qquad (5\text{-}1)$$

The power factor (PF) at which power is drawn is defined as the ratio of the real average power P to the product of the rms voltage and the rms current:

$$PF = \frac{P}{V_s I_s} = \cos\phi \qquad \text{(using Eq. 5-1)} \qquad (5\text{-}2)$$

For a given voltage, from Eq. 5-2, the rms current drawn is

$$I_s = \frac{P}{V_s \cdot PF} \tag{5-3}$$

This shows that the power factor PF and the current I_s are inversely proportional. The current flows through the utility distribution lines, transformers, and so on, causing losses in their resistances. This is the reason why utilities prefer unity power factor loads that draw power at the minimum value of the rms current.

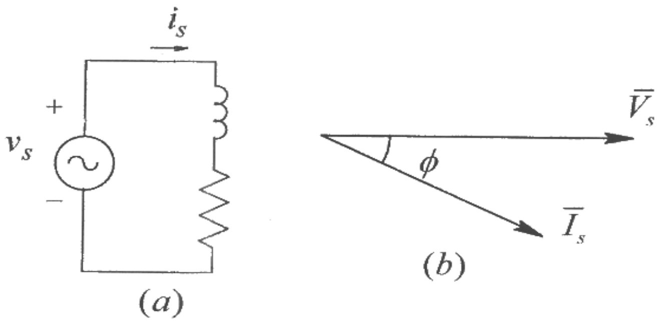


Figure 5-2 Voltage and current phasors in simple *R-L* circuit.

5-2-1 RMS Value of Distorted Current and the Total Harmonic Distortion (*THD*)

The sinusoidal current drawn by the linear load in Fig. 5-2 has zero distortion. However, power electronic systems with diode rectifiers as the front-end draw currents with a distorted waveform such as that shown by $i_s(t)$ in Fig. 5-3a. The utility voltage $v_s(t)$ is assumed sinusoidal. The following analysis is general, applying to the utility supply that is either single-phase or three-phase, in which case the analysis is on a per-phase basis.

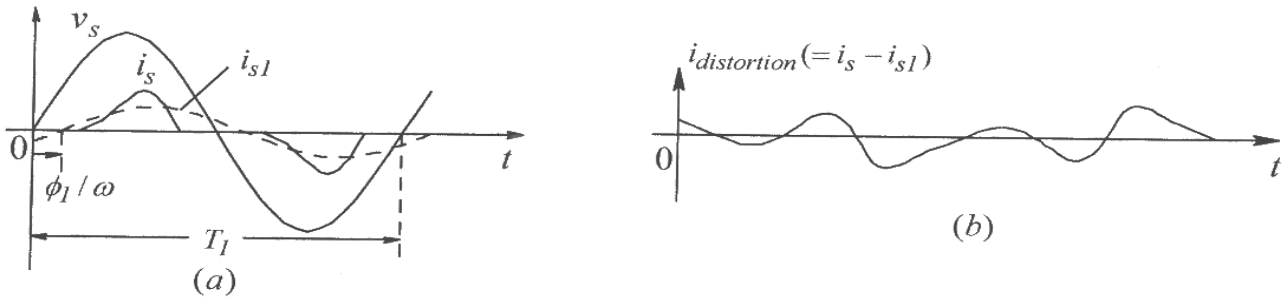


Figure 5-3 Current drawn by power electronics equipment with diode-bridge front-end.

The current waveform $i_s(t)$ in Fig. 5-3a repeats with a time-period T_1. By Fourier analysis of this repetitive waveform, we can compute its fundamental frequency $(=1/T_1)$ component $i_{s1}(t)$, shown dotted in Fig. 5-3a. The distortion component $i_{distortion}(t)$ in the input current is the difference between $i_s(t)$ and the fundamental-frequency component $i_{s1}(t)$:

$$i_{distortion}(t) = i_s(t) - i_{s1}(t) \tag{5-4}$$

where $i_{distortion}(t)$ using Eq. 5-4 is plotted in Fig. 5-3b. This distortion component consists of components at frequencies that are the multiples of the fundamental frequency.

To obtain the rms value of $i_s(t)$ in Fig. 5-3a, we will apply the basic definition of rms:

$$I_s = \sqrt{\frac{1}{T_1}\int_{T_1} i_s^2(t)\cdot dt} \tag{5-5}$$

Using Eq. 5-4,

$$i_s^2(t) = i_{s1}^2(t) + i_{distortion}^2(t) + 2i_{s1}(t)\times i_{distortion}(t) \tag{5-6}$$

In a repetitive waveform, the integral of the products of the two harmonic components (including the fundamental) at unequal frequencies, over the repetition time-period, equals zero:

$$\int_{T_1} f_{h_1}(t)\cdot g_{h_2}(t)\cdot dt = 0 \qquad\qquad h_1 \neq h_2 \tag{5-7}$$

Therefore, substituting Eq. 5-6 into Eq. 5-5, and making use of Eq. 5-7 that implies that the integral of the third term on the right side of Eq. 5-6 equals zero,

$$I_s = \sqrt{\underbrace{\frac{1}{T_1}\int_{T_1} i_{s1}^2(t)\cdot dt}_{I_{s1}^2} + \underbrace{\frac{1}{T_1}\int_{T_1} i_{distortion}^2(t)\cdot dt}_{I_{s1}^2} + 0} \tag{5-8}$$

or,

$$I_s = \sqrt{I_{s1}^2 + I_{distortion}^2} \tag{5-9}$$

where the rms values of the fundamental-frequency component and the distortion component are as follows:

$$I_{s1} = \sqrt{\frac{1}{T_1}\int_{T_1} i_{s1}^2(t)\cdot dt} \tag{5-10}$$

and

$$I_{distortion} = \sqrt{\frac{1}{T_1}\int_{T_1} i_{distortion}^2(t)\cdot dt} \tag{5-11}$$

Based on the rms values of the fundamental and the distortion components in the input current $i_s(t)$, a distortion index called the Total Harmonic Distortion (*THD*) is defined in percentage as follows:

$$\%THD = 100 \times \frac{I_{distortion}}{I_{s1}} \tag{5-12}$$

Using Eq. 5-9 into Eq. 5-12,

$$\%THD = 100 \times \frac{\sqrt{I_s^2 - I_{s1}^2}}{I_{s1}} \tag{5-13}$$

The rms value of the distortion component can be obtained based on the harmonic components (except the fundamental) as follows using Eq. 5-7:

$$I_{distortion} = \sqrt{\sum_{h=2}^{\infty} I_{sh}^2} \tag{5-14}$$

where I_{sh} is the rms value of the harmonic component "h".

▲ **Example 5-1** A current i_s of square waveform is shown in Fig. 5-4a. Calculate and plot its fundamental frequency component and its distortion component. What is the %*THD* associated with this waveform?

Solution From Fourier analysis, $i_s(t)$ can be expressed as

$$i_s = \frac{4}{\pi} I(\sin \omega_1 t + \frac{1}{3}\sin 3\omega_1 t + \frac{1}{5}\sin 5\omega_1 t + \frac{1}{7}\sin 7\omega_1 t + ...) \tag{5-15}$$

The fundamental frequency component and the distortion component are plotted in Figs. 5-4b and 5-4c.

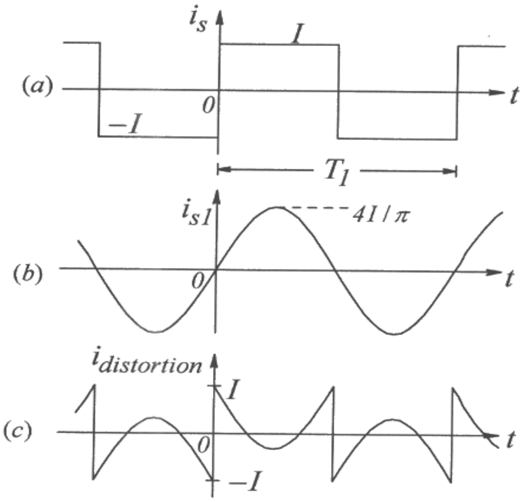


Figure 5-4 Example 5-1.

Since the rms value I_s of the square waveform is equal to I, the rms value of the distortion component can be calculated from using Eq. 5-9 in Eq. 5-15

$$I_{distortion} = \sqrt{I_s^2 - I_{s1}^2} = \sqrt{I^2 - (0.9I)^2} = 0.436I .$$

Therefore, using the definition of *THD*,

$$\% THD = 100 \times \frac{I_{distortion}}{I_{s1}} = 100 \times \frac{0.436I}{0.9I} = 48.4\% .$$ ▲

5-2-2 The Displacement Power Factor (*DPF*) and Power Factor (*PF*)

Next, we will consider the power factor at which power is drawn by a load with a distorted current waveform such as that shown in Fig. 5-3a. As before, it is reasonable to assume that the utility-supplied line-frequency voltage $v_s(t)$ is sinusoidal, with an rms value of V_s and a frequency $f_1 (= \frac{\omega_1}{2\pi})$. Based on Eq. 5-7, which states that the product of the cross-frequency terms has a zero average, the average power P drawn by the load in Fig. 5-3a is due only to the fundamental-frequency component of the current:

$$P = \frac{1}{T_1} \int_{T_1} v_s(t) \cdot i_s(t) \cdot dt = \frac{1}{T_1} \int_{T_1} v_s(t) \cdot i_{s1}(t) \cdot dt \tag{5-16}$$

Therefore, in contrast to Eq. 5-1 for a linear load, in a load that draws distorted current, similar to Eq. 5-1

$$P = V_s I_{s1} \cos\phi_1 \tag{5-17}$$

where ϕ_1 is the angle by which the fundamental-frequency current component $i_{s1}(t)$ lags behind the voltage, as shown in Fig. 5-3a.

At this point, another term called the Displacement Power Factor (*DPF*) needs to be introduced, where

$$DPF = \cos\phi_1 \tag{5-18}$$

Therefore, using the *DPF* in Eq. 5-17,

$$P = V_s I_{s1} (DPF) \tag{5-19}$$

In the presence of distortion in the current, the meaning and therefore the definition of the power factor, at which the real average power P is drawn, remains the same as in Eq. 5-2, that is, the ratio of the real power to the product of the rms voltage and the rms current:

$$PF = \frac{P}{V_s I_s} \tag{5-20}$$

Substituting Eq. 5-19 for P into Eq. 5-20,

$$PF = \left(\frac{I_{s1}}{I_s}\right)(DPF) \tag{5-21}$$

In linear loads that draw sinusoidal currents, the current-ratio (I_{s1}/I_s) in Eq. 5-21 is unity, hence $PF = DPF$. Eq. 5-21 shows the following: a high distortion in the current waveform leads to a low power factor, even if the DPF is high. Using Eq. 5-13, the ratio (I_{s1}/I_s) in Eq. 5-21 can be expressed in terms of the Total Harmonic Distortion as

$$\frac{I_{s1}}{I_s} = \frac{1}{\sqrt{1+\left(\frac{\%THD}{100}\right)^2}} \tag{5-22}$$

Therefore, in Eq. 5-21,

$$PF = \frac{1}{\sqrt{1+\left(\frac{\%THD}{100}\right)^2}} \cdot DPF \tag{5-23}$$

The effect of THD on the power factor is shown in Fig. 5-5 by plotting (PF/DPF) versus THD. It shows that even if the displacement power factor is unity, a total harmonic distortion of 100 percent (which is possible in power electronic systems unless corrective measures are taken) can reduce the power factor to approximately 0.7 (or $\frac{1}{\sqrt{2}} = 0.707$ to be exact), which is unacceptably low.

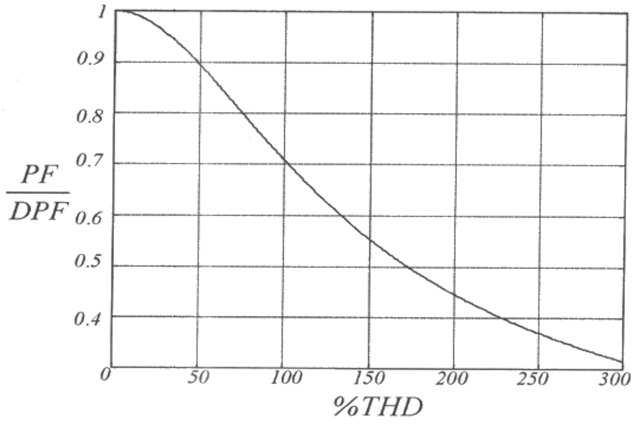


Figure 5-5 Relation between PF/DPF and THD.

5-2-3 Deleterious Effects of Harmonic Distortion and a Poor Power Factor

There are several deleterious effects of high distortion in the current waveform and the poor power factor that results due to it. These are as follows:

- Power loss in utility equipment such as distribution and transmission lines, transformers, and generators increases, possibly to the point of overloading them.
- Harmonic currents can overload the shunt capacitors used by utilities for voltage support and may cause resonance conditions between the capacitive reactance of these capacitors and the inductive reactance of the distribution and transmission lines.
- The utility voltage waveform will also become distorted, adversely affecting other linear loads, if a significant portion of the load supplied by the utility draws power by means of distorted currents.

5-2-3-1 Harmonic Guidelines

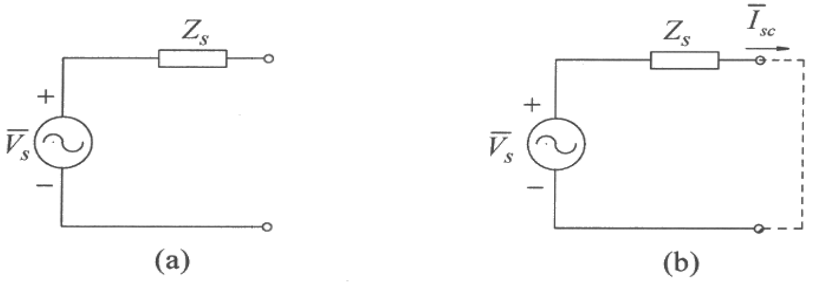
In order to prevent degradation in power quality, recommended guidelines (in the form of the IEEE-519) have been suggested by the IEEE (Institute of Electrical and Electronics Engineers). These guidelines place the responsibilities of maintaining power quality on the consumers and the utilities as follows: 1) on the power consumers, such as the users of power electronic systems, to limit the distortion in the current drawn, and 2) on the utilities to ensure that the voltage supply is sinusoidal with less than a specified amount of distortion.

The limits on current distortion placed by the IEEE-519 are shown in Table 5-1, where the limits on harmonic currents, as a ratio of the fundamental component, are specified for various harmonic frequencies. Also, the limits on the *THD* are specified. These limits are selected to prevent distortion in the voltage waveform of the utility supply.

Table 5-1 Harmonic current distortion (I_h/I_1)

	Odd Harmonic Order h (in %)					*Total Harmonic Distortion(%)*
I_{sc}/I_1	$h<11$	$11 \le h < 17$	$17 \le h < 23$	$23 \le h < 35$	$35 \le h$	
<20	4.0	2.0	1.5	0.6	0.3	5.0
$20-50$	7.0	3.5	2.5	1.0	0.5	8.0
$50-100$	10.0	4.5	4.0	1.5	0.7	12.0
$100-1000$	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Therefore, the limits on distortion in Table 5-1 depend on the "stiffness" of the utility supply, which is shown in Fig. 5-6a by a voltage source $\overline{V}_s$ in series with internal impedance Z_s. An ideal voltage supply has zero internal impedance. In contrast, the voltage supply at the end of a long distribution line, for example, will have large internal impedance.



(a) (b)

Figure 5-6 (a) Utility supply; (b) short circuit current.

To define the "stiffness" of the supply, the short-circuit current I_{sc} is calculated by hypothetically placing short-circuit at the supply terminals, as shown in Fig. 5-6b. The stiffness of the supply must be calculated in relation to the load current. Therefore, the stiffness is defined by a ratio called the Short-Circuit-Ratio *(SCR)*:

$$\text{Short-Circuit-Ratio } SCR = \frac{I_{sc}}{I_{s1}} \tag{5-24}$$

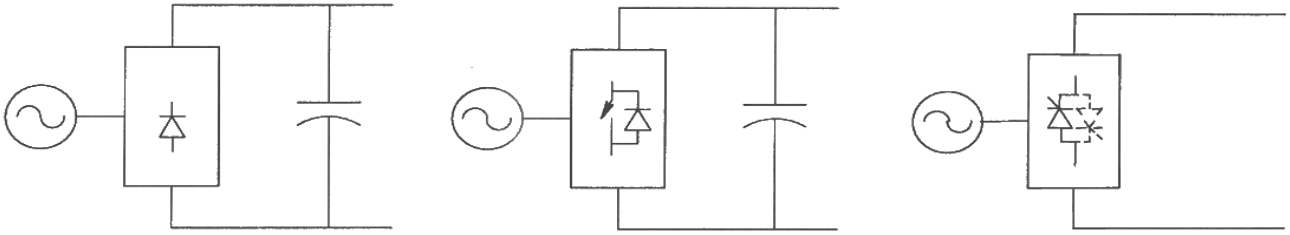
where I_{s1} is the fundamental-frequency component of the load current. Table 5-1 shows that a smaller short-circuit ratio corresponds to lower limits on the allowed distortion in the current drawn. For the short-circuit-ratio of less than 20, the total harmonic distortion in the current must be less than 5 percent. Power electronic systems that meet this limit would also meet the limits of more stiff supplies.

It should be noted that the IEEE-519 does not propose harmonic guidelines for individual pieces of equipment but rather for the aggregate of loads (such as in an industrial plant) seen from the service entrance, which is also the point-of-common-coupling (PCC) with other customers. However, the IEEE-519 is frequently interpreted as the harmonic guidelines for specifying individual pieces of equipment such as motor drives. There are other harmonic standards, such as the IEC-1000, which apply to individual pieces of equipment.

5-3 CLASSIFYING THE "FRONT-END" OF POWER ELECTRONIC SYSTEMS

Interaction between the utility supply and power electronic systems depends on the "front-ends" (within the power-processing units), which convert line-frequency ac into dc. These front-ends can be broadly classified as follows:

- Diode-bridge rectifiers (shown in Fig. 5-7a) in which power flows only in one direction
- Switch-mode converters (shown in Fig. 5-7b) in which the power flow can reverse and the line currents are sinusoidal at the unity power factor
- Thyristor converters (shown in Fig. 5-7c) in which the power flow can be made bi-directional



(*a*) (*b*) (*c*)

Figure 5-7 Front-end of power electronics equipment.

All of these front-ends can be designed to interface with single-phase or three-phase utility systems. In the following discussion, a brief description of the diode interface shown in Fig. 5-7a is provided, supplemented by analysis of results obtained through computer simulations. Interfaces using switch-mode converters in Fig. 5-7b and thyristor converters in Fig. 5-7c are discussed later in this book.

5-4 DIODE-RECTIFIER BRIDGE "FRONT-ENDS"

Most power electronic systems use diode-bridge rectifiers, like the one shown in Fig. 5-7a, even though they draw currents with highly distorted waveforms and the power through them can flow only in one direction. In switch-mode dc power supplies these diode-bridge rectifiers are supplemented by a power-factor-correction circuit, to meet current harmonic limits, as discussed in the next chapter.

Diode rectifiers rectify line-frequency ac into dc across the dc-bus capacitor, without any control over the dc-bus voltage. For analyzing the interaction between the utility and the power electronic systems, the switch-mode converter and the load can be represented by an equivalent resistance R_{eq} across the dc-bus capacitor. In our theoretical discussion, it is adequate to assume the diodes ideal.

In the following subsections, we will consider single-phase as well as three-phase diode rectifiers operating in steady state, where waveforms repeat from one line-frequency cycle $T_1(=1/f_1)$ to the next.

5-4-1 Single-Phase Diode-Rectifier Bridge

At power levels below a few kW, for example in residential applications, power electronic systems are supplied by a single-phase utility source. A commonly used full-bridge rectifier circuit is shown in Fig. 5-8, in which L_s is the sum of the inductance internal to the utility supply and an external inductance, which may be intentionally added in series. Losses on the ac side can be represented by the series resistance R_s.

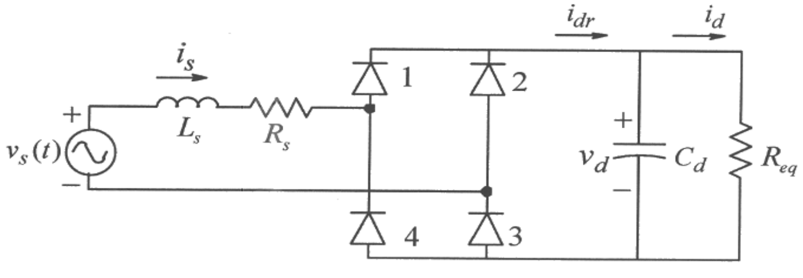


Figure 5-8 Full-bridge diode rectifier.

As shown in Fig. 5-9, at the beginning of the positive half-cycle of the input voltage v_s, the capacitor is already charged to a dc voltage v_d. So long as v_d exceeds the input voltage magnitude, all diodes get reverse biased and the input current is zero. Power to the equivalent resistance R_{eq} is supplied by the energy stored in the capacitor up to t_1. Beyond t_1, the input current $i_s(=i_{dr})$ increases, flowing through diodes D_1 and D_2. Beyond t_2, the input voltage becomes smaller than the capacitor voltage and the input current begins to decline, falling to zero at t_3. Beyond t_3, until one-half cycle later than t_1, the input current remains zero and the power to R_{eq} is supplied by the energy stored in the capacitor.

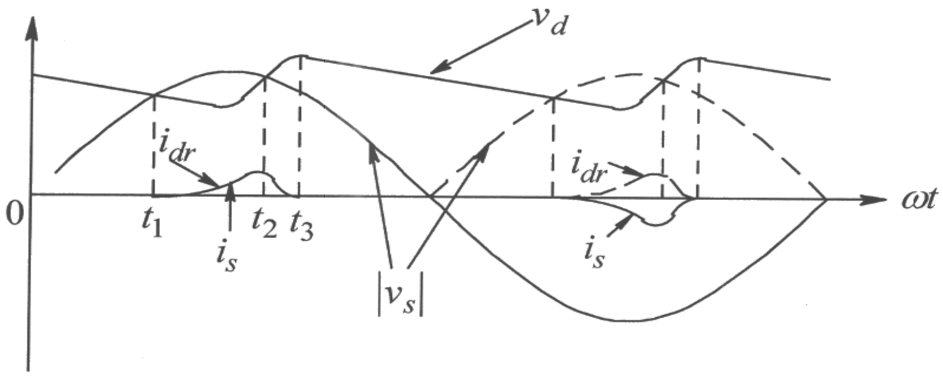


Figure 5-9 Current and voltage waveforms for the full-bridge diode rectifier.

At $(t_1 + \frac{T_1}{2})$ during the negative half-cycle of the input voltage, the input current flows through diodes D_3 and D_4. The rectifier dc-side current i_{dr} continues to flow in the same direction as during the positive half-cycle; however, the input current $i_s = -i_{dr}$, as shown in Fig. 5-9. Fig. 5-10 shows waveforms obtained by PSpice simulations for two values of the ac-side inductance, with current THD of 86% and 62%, respectively (higher inductance reduces THD, as discussed in the next section).

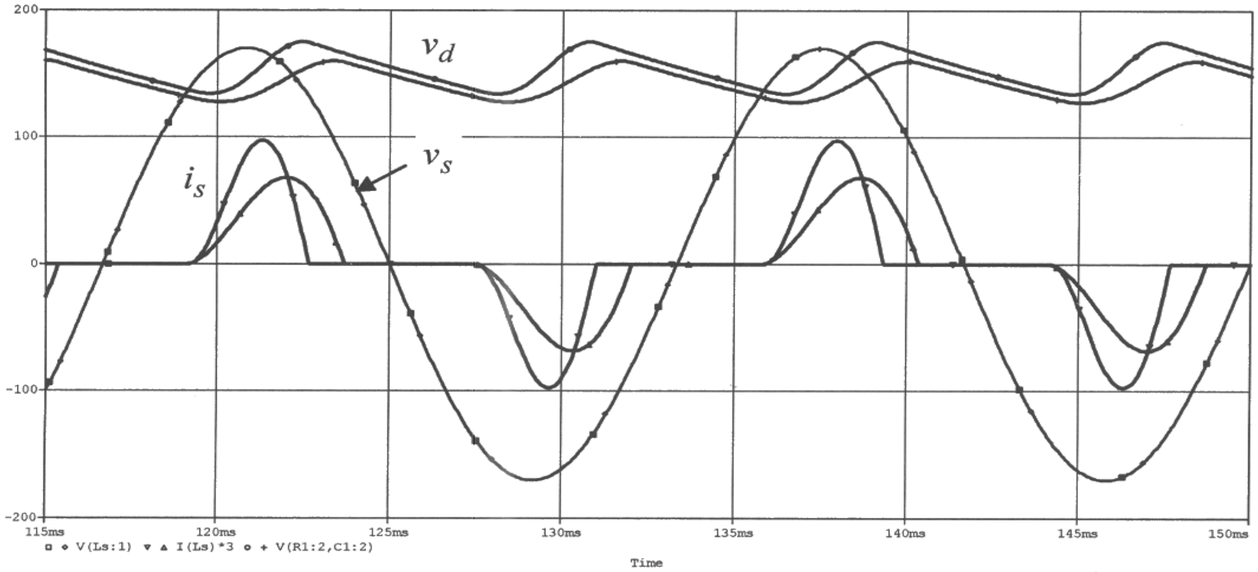


Figure 5-10 Single-phase diode-bridge rectification.

The fact that i_{dr} flows in the same direction during both the positive and the negative half-cycles represents the rectification process. In the circuit of Fig. 5-8 in steady state, all waveforms repeat from one cycle to the next. Therefore, the average value of the capacitor current over a line-frequency cycle must be zero so that the dc-bus voltage is in steady state. As a consequence, the average current through the equivalent load-resistance R_{eq} equals the average of the rectifier dc-side current; that is, $I_d = I_{dr}$.

5-4-1-1 Effects of L_s and C_d on the Waveforms and the *THD*

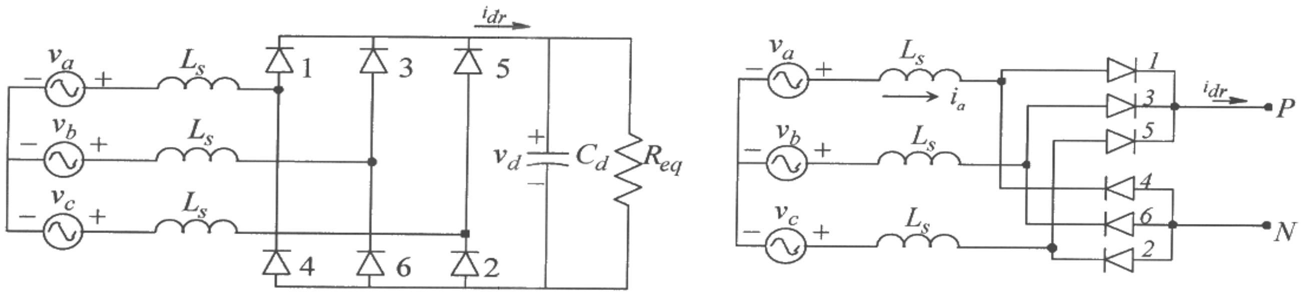
As Figs. 5-9 and 5-10 show, power is drawn from the utility supply by means of a pulse of current every half-cycle. The larger the "base" of this pulse during which the current flows, lower its peak value and the total harmonic distortion (THD). This pulse-widening can be accomplished by increasing the ac-side inductance L_s. Another parameter under the designer's control is the value of the dc-bus capacitor C_d. At its minimum, it should be able to carry the ripple current in i_{dr} and in i_d (which in practice is the input dc-side current, with a pulsating waveform, of a switch-mode converter), and keep the peak-to-peak ripple in the dc-bus voltage to some acceptable value, for example less than 5 percent of the dc-bus average value. Assuming that these constraints are met, lower the value of C_d, lower the *THD* and higher the ripple in the dc-bus voltage.

In practice, it is almost impossible to meet the harmonic limits specified by the IEEE-519 by using the above techniques. Rather, the power-factor-correction circuits described in the next chapter are needed to meet the harmonic specifications.

5-4-2 Three-Phase Diode-Rectifier Bridge

It is preferable to use a three-phase utility source, except at a fractional kilowatt, if such a supply is available. A commonly used Full-Bridge rectifier circuit is shown in Fig. 5-11a.

To understand the circuit operation, the rectifier circuit can be drawn as in Fig. 5-11b. The circuit consists of a top group and a bottom group of diodes. Initially, L_s is ignored and the dc-side current is assumed to flow continuously. At least one diode from each group must conduct to facilitate the flow of i_{dr}. In the top group, all diodes have their cathodes connected together. Therefore, the diode connected to the most positive voltage will conduct; the other two will be reverse biased. In the bottom group, all diodes have their anodes connected together. Therefore, the diode connected to the most negative voltage will conduct; the other two will be reverse biased.



(*a*) (*b*)

Figure 5-11 Three-phase diode bridge rectifier.

Ignoring L_s and assuming that the dc-side current i_{dr} is a pure dc, the waveforms are as shown in Fig. 5-12. In Fig. 5-12a, the waveforms (identified by the dark portions of the curves) show that each diode, based on the principle described above, conducts during 120^0. The diodes are numbered so that they begin conducting sequentially: 1, 2, 3, and so on. The waveforms for the voltages v_P and v_N, with respect to the source-neutral, consist of 120^0-segments of the phase voltages, as shown in Fig. 5-12a. The waveform of the dc-side voltage $v_d(=v_P - v_N)$ is shown in Fig. 5-12b. It consists of 60^0-segments of the line-line voltages supplied by the utility. Line currents on the ac-side are as shown in Fig. 5-12c. For example, phase-a current flows for 120^0 during each half-cycle of the phase-a input voltage; it flows through diode D_1 during the positive half-cycle of v_a, and through diode D_4 during the negative half-cycle.

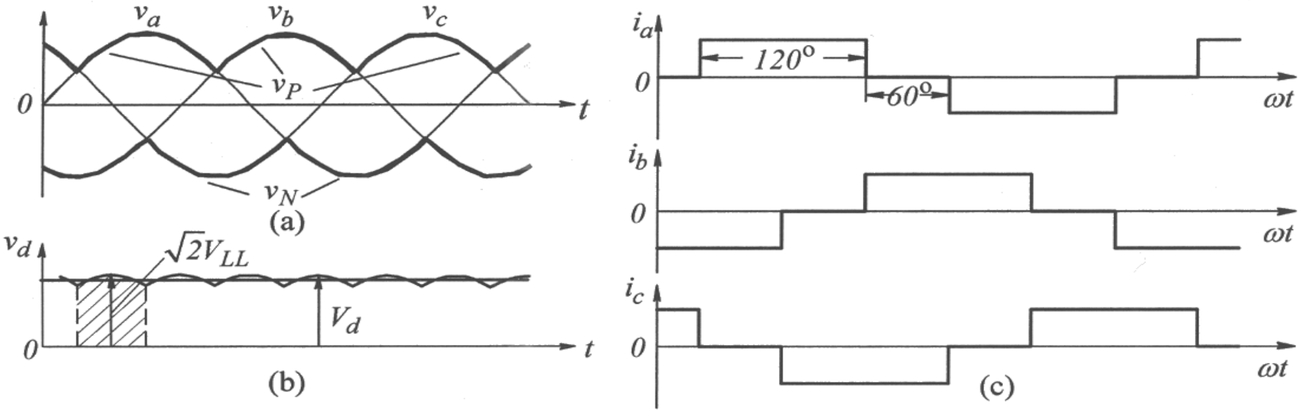


Figure 5-12 Waveforms in a three-phase rectifier (a constant i_{dr}).

The average value of the dc-side voltage can be obtained by considering only a 60^0-segment in the 6-pulse (per line-frequency cycle) waveform shown in Fig. 5-12b. Let us consider the instant of the peak in the 60^0-segment to be the time-origin, with $\hat{V}_{LL}$ as the peak line-line voltage. The average value V_d can be obtained by calculating the integral from $\omega t = -\pi/6$ to $\omega t = \pi/6$ (the area shown by the hatched area in Fig. 5-12b) and then dividing by the interval $\pi/3$:

$$V_d = \frac{1}{\pi/3} \int_{-\pi/6}^{\pi/6} \hat{V}_{LL} \cos\omega t \cdot d(\omega t) = \frac{3}{\pi}\hat{V}_{LL} \tag{5-25}$$

This average value is plotted as a straight line in Fig. 5-12b. In the three-phase rectifier of Fig. 5-11a with the dc-bus capacitor filter, the input current waveforms obtained by computer simulations are shown in Fig. 5-13.

Fig. 5-13a shows that the input current waveform within each half-cycle consists of two distinct pulses when L_s is small. For example, in the i_a waveform during the positive half-cycle, the first pulse corresponds to the flow of dc-side current through the diode pair (D_1, D_6) and then through the diode pair (D_1, D_2). At larger values of L_s, within each half-cycle, the input current between the two pulses does not go to zero, as shown in Fig. 5-13b.

The effects of L_s and C_d on the waveforms can be determined by a parametric analysis, similar to the case of single-phase rectifiers. The *THD* in the current waveform of Fig. 5-13b is much smaller than in Fig. 5-13a (23% versus 82%). The ac-side inductance L_s is required to provide a line-frequency reactance $X_{L_s}(=2\pi f_1 L_s)$ that is typically greater than 2 percent of the base impedance Z_{base}, which is defined as follows:

$$\text{Base Impedance } Z_{base} = 3\frac{V_s^2}{P} \tag{5-26}$$

where P is the three-phase power rating of the power electronic system, and V_s is the rms value of the phase voltage. Therefore, typically, the minimum ac-side inductance should be such that

$$X_{L_s} \geq (0.02 \times Z_{base}) \tag{5-27}$$

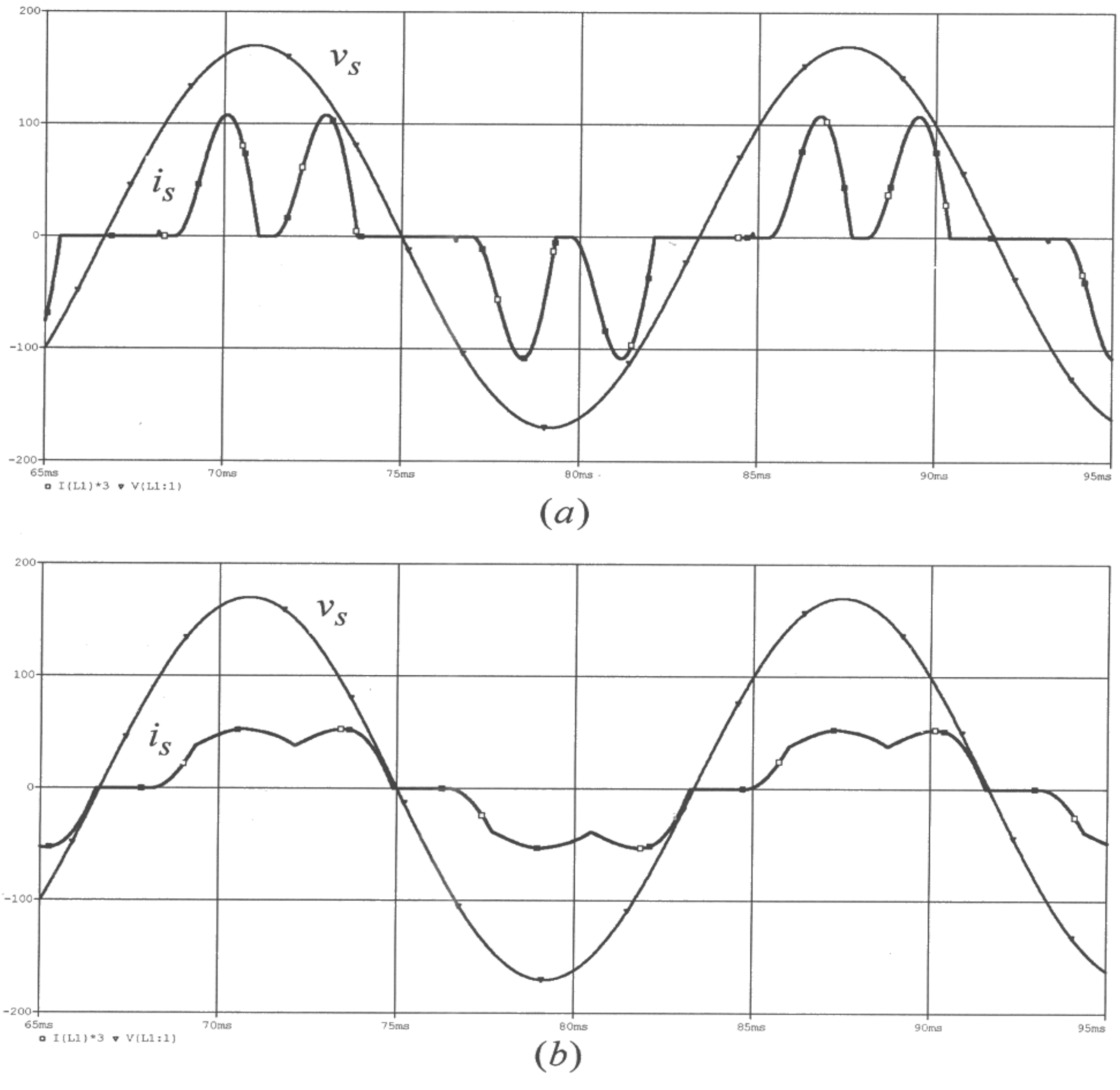


Figure 5-13 Effect of L_s variation (a) $L_s = 0.1 mH$; (b) $L_s = 3 mH$.

5-4-3 Comparison of Single-Phase and Three-Phase Rectifiers

Examination of single-phase and three-phase rectifier waveforms shows the differences in their characteristics. Three-phase rectification results in six identical "pulses" per cycle in the rectified dc-side voltage, whereas single-phase rectification in two such pulses. Therefore, three-phase rectifiers are superior in terms of minimizing distortion in line currents and ripple across the dc-bus voltage. Consequently, as stated earlier, three-phase rectifiers should be used if a three-phase supply is available. However, three-phase rectifiers, just like single-phase rectifiers, are also unable to meet the harmonic limits specified by the IEEE-519 unless corrective actions such as those described in Chapter 12 are taken.

5-5 Means to Avoid Transient Inrush Currents at Starting

In power electronic systems with rectifier front-ends, it may be necessary to take steps to avoid a large inrush of current at the instant the system is connected to the utility source. In such power electronic systems, the dc-bus capacitor is very large and initially has no voltage across it. Therefore, at the instant the switch in Fig. 5-14a is closed to connect the power electronic system to the utility source, a large current flows through the diode-bridge rectifier, charging the dc-bus capacitor.

This transient current inrush is highly undesirable; fortunately, several means of avoiding it are available. These include using a front-end that consists of thyristors discussed in Chapter 14 or using a series semiconductor switch as shown in Fig. 5-14b. At the instant of starting, the resistance across the switch lets the dc-bus capacitor get charged without a large inrush current, and subsequently the semiconductor switch is turned on to bypass the resistance.

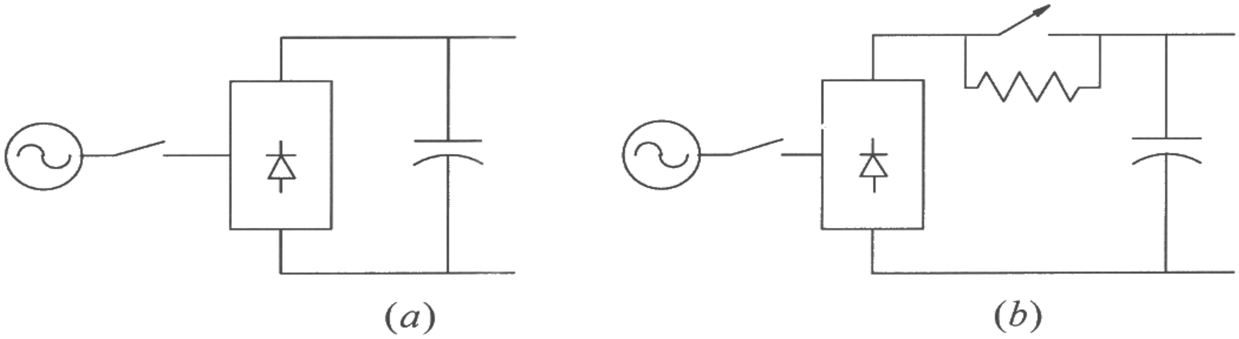


Figure 5-14 Means to avoid inrush current.

5-6 FRONT-ENDS WITH BI-DIRECTIONAL POWER FLOW

In stop-and-go applications such as elevators, it is cost-effective to feed the energy recovered by regenerative braking of the motor drive back into the utility supply. Converter arrangements for such applications are considered in Chapter 12.

REFERENCES

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.
2. N. Mohan, Power Electronics: *Computer Simulation, Analysis and Education using PSpice*™, a complete simulation package available from www.mnpere.com.

PROBLEMS

5-1 In a single-phase diode rectifier bridge, $I_s = 10\,A(rms)$, $I_{s1} = 8\,A(rms)$, and $DPF = 0.9$. Calculate $I_{distortion}$ and $\%THD$.

5-2 In a single-phase diode bridge rectifier circuit, the following operating condition are given: $V_s = 120\,V(rms)$, $P = 1\,kW$, $I_{s1} = 10\,A$, and $THD = 80\%$. Calculate the following: DPF, $I_{distortion}$, I, and PF.

5-3 In a single-phase rectifier the input current can be approximated to have a triangular waveform every half cycle with a peak of $10\,A$ and a base of 60^0. Calculate the rms current through each diode.

5-4 In the above problem, calculate the ripple component in the dc-side current that will flow through the dc-side capacitor.

5-5 Repeat Example 5-1 if the current waveform is a rectangular pulse as shown in Fig 5-12c in a three-phase rectifier, with an amplitude of $10\,A$.

Chapter 6

POWER-FACTOR-CORRECTION (PFC) CIRCUITS AND DESIGNING THE FEEDBACK CONTROLLER

6-1 INTRODUCTION

Technical solutions to the problem of distortion in the input current have been known for a long time. However, only recently has the concern about the deleterious effects of harmonics led to the formulation of guidelines and standards, which in turn have focused attention on ways of limiting current distortion.

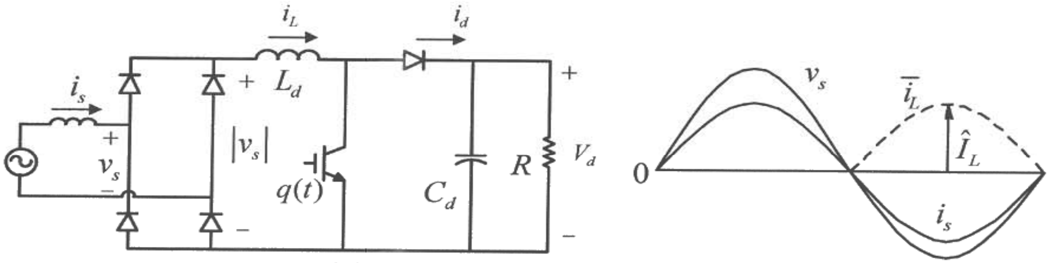
In the following sections, power-factor-corrected (*PF*C) interface, as they are often called, are briefly examined for single-phase rectification, where it is assumed that the power needs to flow only in one direction, such as in dc power supplies. The three-phase front-ends in motor-drives applications may require bi-directional power flow capability. Such front-ends, which also allow unity power factor of operation, are discussed in Chapter 12.

6-2 OPERATING PRINCIPLE OF SINGLE-PHASE *PF*Cs

Operating principle of a commonly used single-phase *PF*C is shown in Fig. 6-1a where, between the utility supply and the dc-bus capacitor, a Boost dc-dc converter is introduced. This Boost converter consists of a MOSFET, a diode, and a small inductor L_d. By pulse-width-modulating the MOSFET at a constant switching frequency, the current i_L through the inductor L_d is shaped to have the full-wave-rectified waveform $|\sin \omega t|$, similar to $|v_s(t)|$, as shown in Fig. 6-1b. The inductor current contains high switching-frequency ripple, which is removed by a small filter, and the input current i_s is sinusoidal, and in phase with the supply voltage. In the Boost converter, it is essential that the dc-bus voltage V_d be greater than the peak of the supply voltage $\hat{V}_s$:

$$V_d > \hat{V}_s \tag{6-1}$$

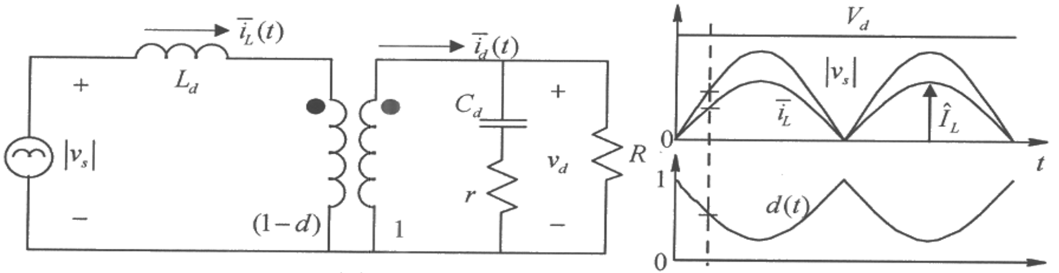
Using the average model of the Boost converter as shown in Fig. 6-2a and neglecting a small voltage drop across the inductor and assuming the voltage across the capacitor to be a pure dc,



i_L
i_d
i_s
L_d
v_s
$|v_s|$
$q(t)$
C_d
R
V_d
+
-
v_s
$\overline{i}_L$
$\hat{I}_L$
i_s
0

(a) (b)

Figure 6-1 PFC circuit and waveforms.



$\overline{i}_L(t)$
$\overline{i}_d(t)$
L_d
$|v_s|$
$(1-d)$
1
C_d
r
v_d
R
+
-
V_d
$|v_s|$
$\overline{i}_L$
$\hat{I}_L$
$d(t)$
0
1
t_1
t

(a) (b)

Figure 6-2 Average model and waveforms.

$$\frac{V_d}{|v_s|}=\frac{1}{1-d(t)} \tag{6-2}$$

thus,

$$d(t)=1-\frac{\hat{V}_s|\sin(\omega t)|}{V_d} \tag{6-3}$$

The switch duty-ratio in the average circuit of Fig. 6-2a is plotted in Fig. 6-2b. The output-stage current $\overline{i}_d(t)$ can be calculated from the ideal transformer in Fig. 6-2a in terms of $|v_s|=\hat{V}_s|\sin\omega t|$ and $\overline{i}_L(t)=\hat{I}_L|\sin\omega t|$, and by using Eq. 6-2,

$$\overline{i}_d(t)=(1-d)\overline{i}_L(t)=\frac{\hat{V}_s}{V_d}\hat{I}_L|\sin\omega t|^2 \tag{6-4}$$

Recognizing that in Eq. 6-4, $|\sin\omega t|^2=\sin^2\omega t=\frac{1}{2}-\frac{1}{2}\cos 2\omega t$:

$$\overline{i}_d=\underbrace{\frac{1}{2}\frac{\hat{V}_s}{V_d}\hat{I}_L}_{I_d}-\underbrace{\frac{1}{2}\frac{\hat{V}_s}{V_d}\hat{I}_L\cos 2\omega t}_{i_{d2}(t)} \tag{6-5}$$

Eq. 6-5 shows that the average current to the output stage consists of a dc component I_d and a component $i_{d2}(t)$ at the second-harmonic component. In PFCs, the capacitor in the output stage shown in Fig. 6-3 is quite large such that it is justifiable to approximate that all the second-harmonic ripple flows through the output capacitor, and only I_d flows through the load equivalent resistor. Based on this assumption, the second-harmonic ripple in the output voltage can be calculated as

$$v_{d2}(t) = \frac{1}{\omega C}\int i_{d2}\cdot d(\omega t) \tag{6-6}$$

Substituting i_{d2} from Eq. 6-5 into Eq. 6-6,

$$v_{d2} = -\frac{1}{\omega C}\frac{\hat{I}_L}{2}\frac{\hat{V}_s}{V_d}\int \cos 2\omega t \cdot d(\omega t) = -\underbrace{\left(\frac{\hat{I}_L \hat{V}_s}{4\omega C V_d}\right)}_{\hat{V}_{d2}}\sin 2\omega t \tag{6-7}$$

where

$$\hat{V}_{d2} = \frac{\hat{I}_L}{4\omega C}\frac{\hat{V}_s}{V_d} \tag{6-8}$$

is the peak value of the ripple in the output capacitor. It depends inversely on the output capacitance, and therefore an appropriate value must be chosen to minimize this ripple.

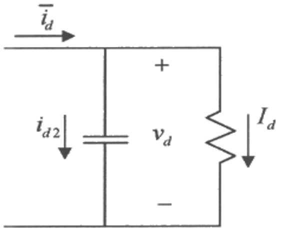


Figure 6-3 Current division in the output stage.

6-3 CONTROL OF PFCs

In controlling a PFC, the main objective is to draw a sinusoidal current, in-phase with the utility voltage. The reference inductor current $i_L^*(t)$ is of the full-wave rectified form, similar to that in Fig. 6-1b. The requirements on the form and the amplitude of the inductor current lead to two control loops, as shown in Fig. 6-4, to pulse-width modulate the switch of the Boost converter:

- The inner current loop ensures the form of $i_L^*(t)$ based on the utility voltage $v_s(t)$.
- The outer voltage loop determines the amplitude $\hat{I}_L$ of $i_L^*(t)$ based on the output voltage feedback. If the inductor current is insufficient for a given load supplied by the PFC, the output voltage will drop below its pre-selected reference value V_d^*. By measuring the output voltage and using it as the feedback signal, the voltage loop adjusts the inductor current amplitude to bring the output voltage to

its reference value. In addition to determining the inductor current amplitude, this voltage feedback control acts to regulate the output voltage of the PFC to the pre-selected dc voltage.

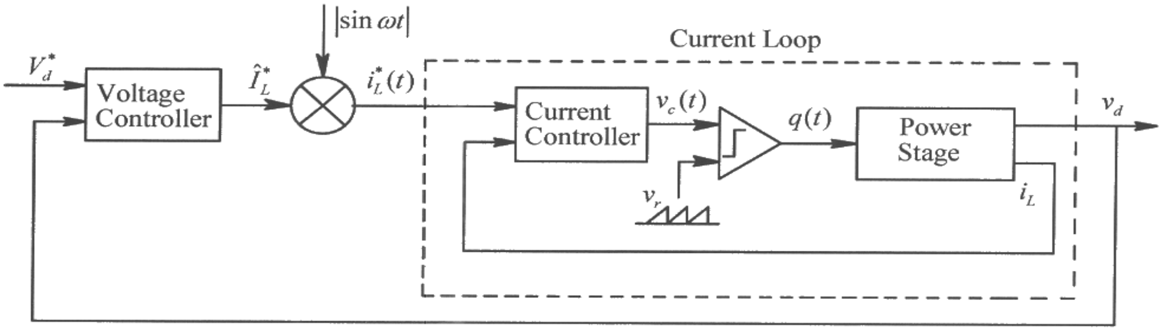


Figure 6-4 PFC control loops.

Fortunately, in Fig. 6-4, the inner current loop is required to have a very high bandwidth compared to the outer voltage loop. Hence, each loop can be designed separately, similar to the approach taken in the peak-current-mode control discussed Chapter 4.

6-4 DESIGNING THE INNER AVERAGE-CURRENT-CONTROL LOOP

The inner current loop is shown within the dotted box in Fig. 6-4. In order to follow the reference with as little THD as possible, an average-current-mode control is used with a high bandwidth, where the error between the reference $i_L^*(t)$ and the measured inductor current $i_L(t)$ is amplified by a current controller to produce the control voltage $v_c(t)$. This control voltage is compared with a ramp signal $v_r(t)$, with a peak of $\hat{V}_r$ at the switching-frequency f_s in the PWM controller IC [1], to produce the switching signal $q(t)$.

Just the inner current loop of Fig. 6-4 can be simplified, as shown in Fig. 6-5a. The reference input $i_L^*(t)$ varies with time as shown in Fig. 6-2b, where the corresponding $v_s(t)$ and $d(t)$ waveforms are also plotted. However, these quantities vary much more slowly compared to the control-loop bandwidth, approximately 10 *kHz* in the numerical example considered later on. Therefore, at each instant of time, for example at t_1 in Fig. 6-2b, the circuit of Fig. 6-2a can be considered in a "dc" steady state with the associated variables having values of $i_L(t_1)$, $v_s(t_1)$ and $d(t_1)$. This equilibrium condition slowly varies with time, and the current loop is designed to have a large bandwidth around each dc steady state. In Laplace domain, this current loop is shown in Fig. 6-5b, as discussed below, where "~" on top represents small signal perturbations at very high frequencies in the range of the current-loop bandwidth, for example 10 kHz.

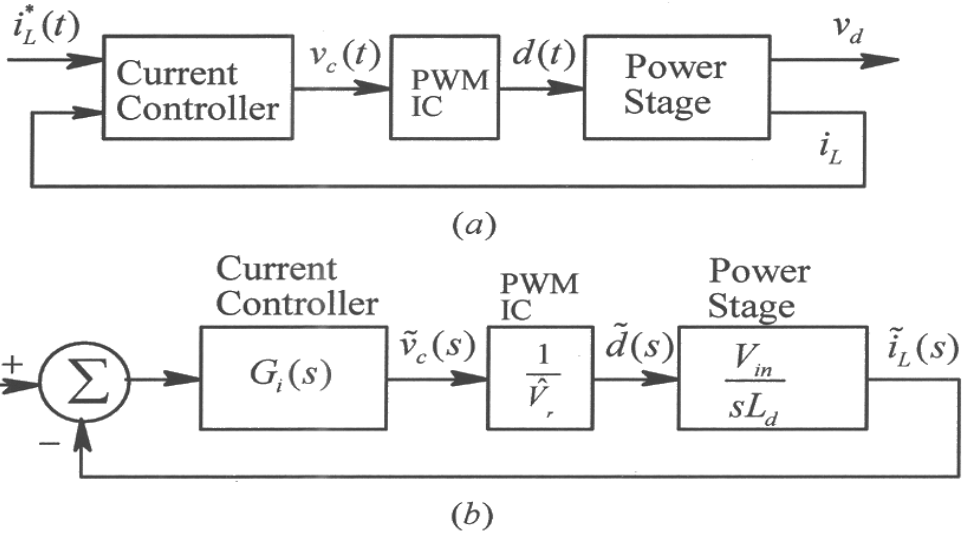

$i_L^*(t)$
Current Controller
$v_c(t)$
PWM IC
$d(t)$
Power Stage
v_d
i_L
(a)
Current Controller
PWM IC
Power Stage
$\tilde{i}_L^*(s)$
+
−
Σ
$G_i(s)$
$\tilde{v}_c(s)$
$\frac{1}{\hat{V}_r}$
$\tilde{d}(s)$
$\frac{V_{in}}{sL_d}$
$\tilde{i}_L(s)$
(b)

Figure 6-5 PFC current loop.

6-4-1 $\tilde{d}(s)/\tilde{v}_c(s)$ for the PWM Controller

If $\hat{V}_r$ is the difference between the peak and the valley of the ramp voltage in the PWM-IC, then the small-signal transfer function of the PWM controller, as discussed in Chapter 4 is

$$\text{PWM Controller Transfer Function } \frac{\tilde{d}(s)}{\tilde{v}_c(s)} = \frac{1}{\hat{V}_r} \qquad (6\text{-}9)$$

6-4-2 $\tilde{i}_L(s)/\tilde{d}(s)$ for the Boost Converter in the Power Stage

As described in the Appendix on the accompanying CD, in spite of the varying dc steady state operating point, the transfer function in the Boost converter simplifies as follows at high frequencies, where the current loop has likely to have its bandwidth:

$$\frac{\tilde{i}_L(s)}{\tilde{d}(s)} \simeq \frac{V_d}{sL_d} \qquad (6\text{-}10)$$

6-4-3 Designing the Current Controller $G_i(s)$

The transfer function in Eq. 6-10 is an approximation valid at high frequencies, and not a pure integrator. Therefore, to have a high loop dc gain and a zero dc steady state error in Fig. 6-5b, the current controller transfer function $G_i(s)$ must have a pole at the origin. In the loop in Fig. 6-5b, the phase due to the pole at origin in $G_i(s)$ and that of the power-stage transfer function (Eq. 6-10) add up to -180^0. Hence, $G_i(s)$, as in the peak-current mode control discussed in Chapter 4, includes a pole-zero pair that provides a phase boost, and hence the specified phase margin, for example 60^0 at the loop crossover frequency:

$$G_i(s) = \frac{k_c}{s} \underbrace{\frac{1+s/\omega_z}{1+s/\omega_p}}_{\text{phase boost}} \tag{6-11}$$

where, k_c is the amplifier gain. Knowing the phase boost, ϕ_{boost}, we can calculate the pole-zero locations to provide the necessary phase boost, as discussed in Chapter 4:

$$K_{boost} = \tan(45^o + \frac{\phi_{boost}}{2}) \tag{6-12}$$

$$f_z = \frac{f_{ci}}{K_{boost}} \tag{6-13}$$

$$f_p = K_{boost} f_{ci} \tag{6-14}$$

where f_{ci} is the crossover frequency of the current loop transfer function.

6-5 DESIGNING THE OUTER VOLTAGE LOOP

As mentioned earlier, the outer voltage loop is needed to determine the peak , $\hat{I}_L$, of the inductor current. In this voltage loop, the bandwidth is limited to approximately 15 Hz. The reason has to do with the fact that the output voltage across the capacitor contains a component v_{d2} as derived in Eq. 6-7 at twice the line-frequency (at 120 Hz in 60-Hz line-frequency systems). This output voltage ripple must not be corrected by the voltage loop, otherwise it will lead to third-harmonic distortion in the input current, as explained in the Appendix on the accompanying CD.

In view of such a low bandwidth of the voltage loop (approximately three orders of magnitude below the current-loop bandwidth of ~10 kHz), it is perfectly reasonable to assume the current loop ideal at low frequencies around 15 Hz. Therefore, in the voltage-control block diagram shown in Fig. 6-6a, the current closed-loop produces $\hat{I}_L$ equal to its reference value $\hat{I}_L^*$. In addition to a large dc component, $\hat{I}_L^*$ contains an unwanted second-harmonic component $\hat{I}_{L2}$ due to v_{d2} (Eq. 6-7) in the input to the voltage controller. $\hat{I}_{L2}$ at the second-harmonic component results in a third-harmonic distortion in the current drawn from the utility, as explained in the Appendix on the accompanying CD. Therefore, in the output of the voltage controller block in Fig. 6-6a, $\hat{I}_{L2}$ is limited to approximately 1.5% of the dc component in $\hat{I}_L^*$.

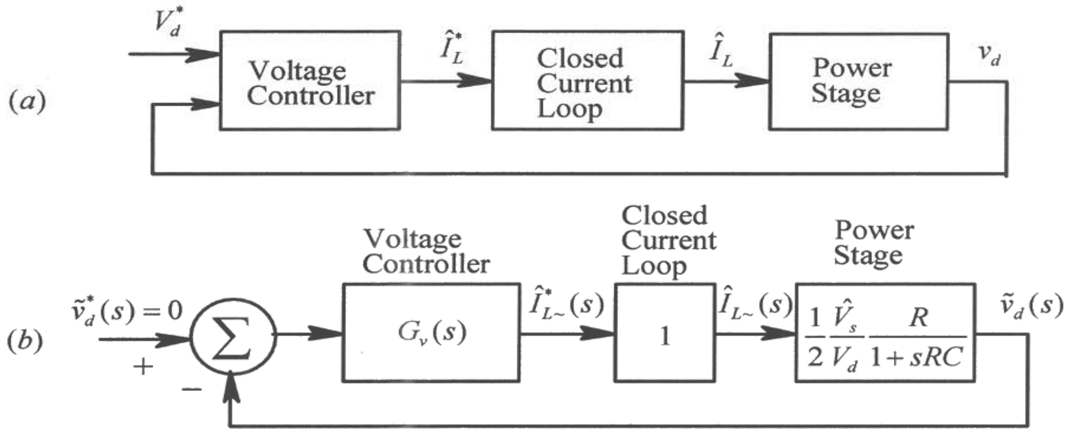

(a)
V_d^*
Voltage Controller
$\hat{I}_L^*$
Closed Current Loop
$\hat{I}_L$
Power Stage
v_d
(b)
$\tilde{v}_d^*(s)=0$
+
−
Σ
Voltage Controller
$G_v(s)$
$\hat{I}_{L\sim}^*(s)$
Closed Current Loop
1
$\hat{I}_{L\sim}(s)$
Power Stage
$\frac{1}{2}\frac{\hat{V}_s}{V_d}\frac{R}{1+sRC}$
$\tilde{v}_d(s)$

Figure 6-6 Voltage control loop.

The voltage control loop for low-frequency perturbations, in the range of the voltage-loop bandwidth of approximately 15 Hz, is shown in Fig. 6-6b. As derived in the Appendix on the accompanying CD, the transfer function of the power stage in Fig. 6-6b at these low perturbation frequencies (ignoring the capacitor ESR) is:

$$\frac{\tilde{v}_d(s)}{\hat{I}_{L\sim}(s)}=\frac{1}{2}\frac{\hat{V}_s}{V_d}\frac{R}{1+sRC} \tag{6-15}$$

To achieve a zero steady state error, the voltage-controller transfer function should have a pole at the origin. However, since the PFC circuit is often a pre-regulator (not a strict regulator), this requirement is waived, which otherwise would make the voltage controller design much more complicated. The following simple transfer function is often used for the voltage controller in Fig. 6-6b, where a pole is placed at the voltage-loop crossover frequency ω_{cv} (yet to be determined) below 15 Hz

$$G_v(s)=\frac{k_v}{1+s/\omega_{cv}} \tag{6-16}$$

At full-load, the power stage transfer function given by Eq. 6-15 has a pole at a very low frequency, for example of the order of one or two Hz, which introduces a phase lag approaching 90 degrees much beyond the frequency at which this pole occurs. The transfer function of the controller given by Eq. 6-16 introduces a lag of 45 degrees at the loop crossover frequency. Therefore, these two phase lags of $\sim 135^0$ at the crossover frequency result in a satisfactory phase margin of 45^0. By definition, at the crossover frequency f_{cv}, the loop transfer function has a magnitude equal to unity

$$\left|\frac{k_v}{1+s/\omega_{cv}}\frac{1}{2}\frac{\hat{V}_s}{V_d}\frac{R}{1+sRC}\right|_{f_{cv}}=1 \tag{6-17}$$

At the second-harmonic in the voltage controller of Eq. 6-16,

$$\left|\frac{k_v}{1+s/\omega_{cv}}\right|_{s=j(2\pi\times 120)} = \frac{\hat{I}_{L2}}{\hat{V}_{d2}} \tag{6-18}$$

From Eqs. 6-17 and 6-18, the two unknowns k_v and ω_{cv} in the voltage controller transfer function of Eq. 6-16 can be calculated, as described by a numerical example.

6-6 EXAMPLE OF SINGLE-PHASE PFC SYSTEMS

The operation and control of a PFC is demonstrated by means of an example, where the parameters are as follows in Table 6-1, and the total harmonic distortion in the input line current is required to be less than 3 percent [1, 2]:

Table 6-1

Parameters and Operating Values

Nominal input ac source voltage, $V_{s,rms}$	$120V$
Line frequency, f	60 Hz
Output Voltage, V_d	$250V$ (dc)
Maximum Power Output	$250W$
Switching Frequency, f_s	$100\,kHz$
Output Filter capacitor, C	$220\,\mu F$
ESR of the Capacitor, r	$100\,m\Omega$
Inductor, L_d	$1\,mH$
Full-Load Equivalent Resistance, R	250Ω

6-6-1 Design of the Current Loop

In Eq. 6-9, $\hat{V}_r$ is given as unity. Following the procedure described in Chapter 4 for the peak-current-mode control of dc-dc converters, for the loop crossover frequency of 10 kHz ($\omega_{ci} = 2\pi\times 10^4$ rad/s) and the phase margin of 60^0, the parameters in the current controller of Eq. 6-11 are as follows:

$$\begin{aligned} k_c &= 4212 \\ \omega_z &= 1.68\times 10^4 rad/s \\ \omega_p &= 2.35\times 10^5 rad/s \end{aligned} \tag{6-19}$$

Based on these parameter values given in Eq. 6-19 of the transfer function $G_i(s)$ in Eq. 6-11, the op-amp circuit is similar to Fig. 4-19 in Chapter 4 with the following values for a chosen value of $R_1 = 100k\Omega$:

$$\begin{aligned} C_2 &\simeq 0.17n\text{F} \\ C_1 &\simeq 2.2n\text{F} \\ R_2 &\simeq 27k\Omega \end{aligned} \tag{6-20}$$

6-6-2 Design of the Voltage Loop

In this example at full-load, the plant transfer function given by Eq. 6-15 has a pole at the frequency of 18.18 rad/s (2.89 Hz). At full-load, $\hat{I}_L = 2.946A$, and in Eq. 6-8, $\hat{V}_{d2} = 6.029V$. Based on the previous discussion, the second-harmonic component is limited to 1.5 percent of $\hat{I}_L$, such that $\hat{I}_{L2} = 0.0442A$. Using these values, from Eq. 6-17 and 6-18, the parameters in the voltage controller transfer function of Eq. 6-16 are calculated: $k_v = 0.0722$, and $\omega_{cv} = 76.634 rad/s$ (12.2 Hz). This transfer function is realized by an op-amp circuit shown in Fig. 6-7 with the following values:

$$\begin{aligned} R_1 &= 100k\Omega \\ R_2 &= 7.2k\Omega \\ C_1 &= 1.8\mu\text{F} \end{aligned} \tag{6-21}$$

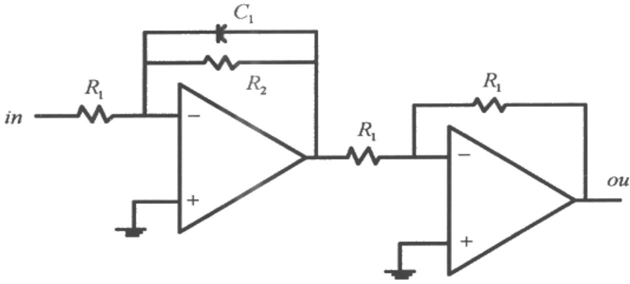


Figure 6-7 Op-amp circuit to implement transfer function $G_v(s)$.

6-7 SIMULATION RESULTS

The PSpice-based simulation of the *PFC* system is shown in Fig. 6-8, where the input voltage and the full-bridge rectifier are combined for simplification purposes. The output load is decreased as a step at 100 ms. The resulting waveforms for the voltage and the inductor current are shown in Fig. 6-9.

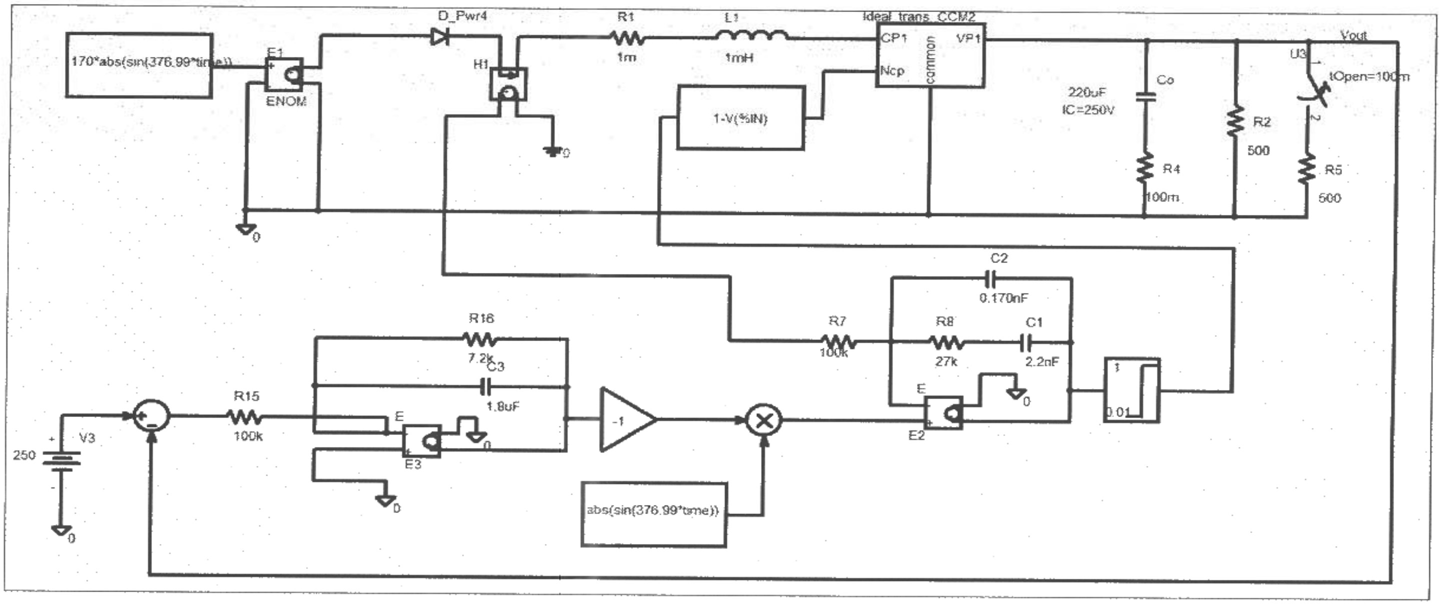

170*abs(sin(376.99*time))
E1
ENOM
D_Pwr4
H1
R1
1m
L1
1mH
ideal_trans_CCM2
CP1
VP1
Ncp
common
1-V(%IN)
220uF
IC=250V
Co
R4
100m
R2
500
U3
tOpen=100m
R5
500
Vout
C2
0.170nF
R7
100k
R8
27k
C1
2.2nF
E
E2
1
0.01
R16
7.2k
C3
1.8uF
R15
100k
E
E3
-1
abs(sin(376.99*time))
V3
250
0

Figure 6-8 PSpice simulation diagram (the load is decreased at 100 ms).

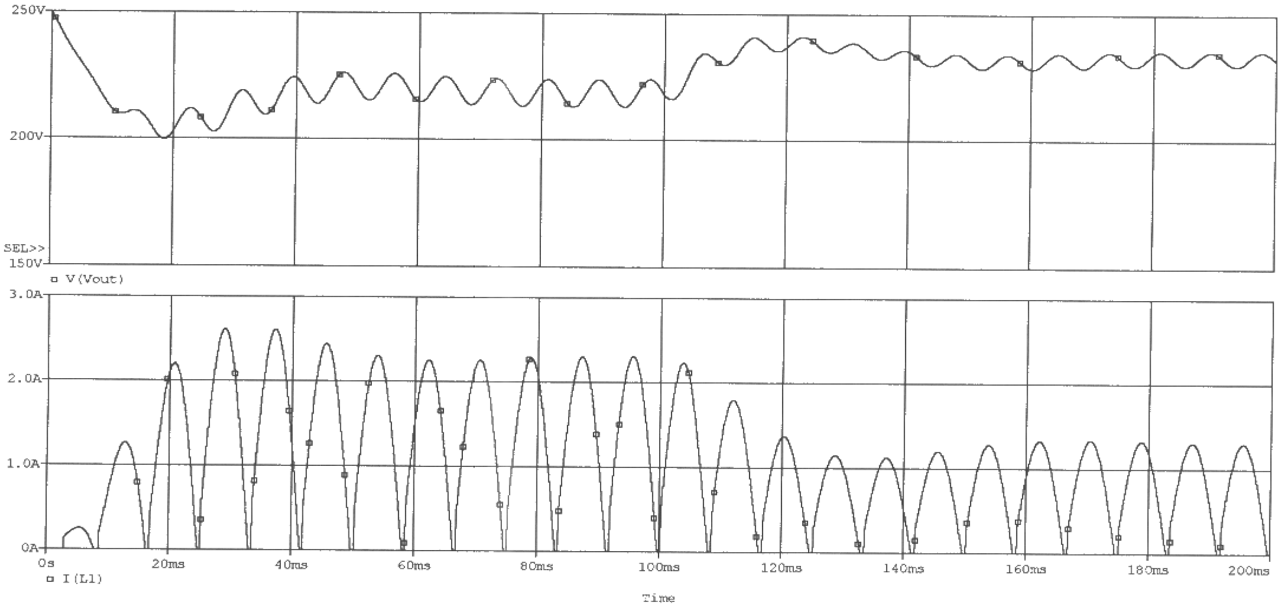


Figure 6-9 Simulation results: output voltage and inductor current.

6-8 FEEDFORWARD OF THE INPUT VOLTAGE

The input voltage is fed forward as shown in Fig. 6-10. In a system with a PFC interface, the output is nearly constant, independent of the changes in the rms value of the input voltage from the utility. Therefore, an increase in the utility voltage $\hat{V}_s$ causes a decrease in $\hat{I}_L$, and vice versa. To avoid propagating the input voltage disturbance though the *PFC* feedback loops, the input voltage peak is fed forward, as shown in Fig. 6-10, in determining $\hat{I}_L^*$.

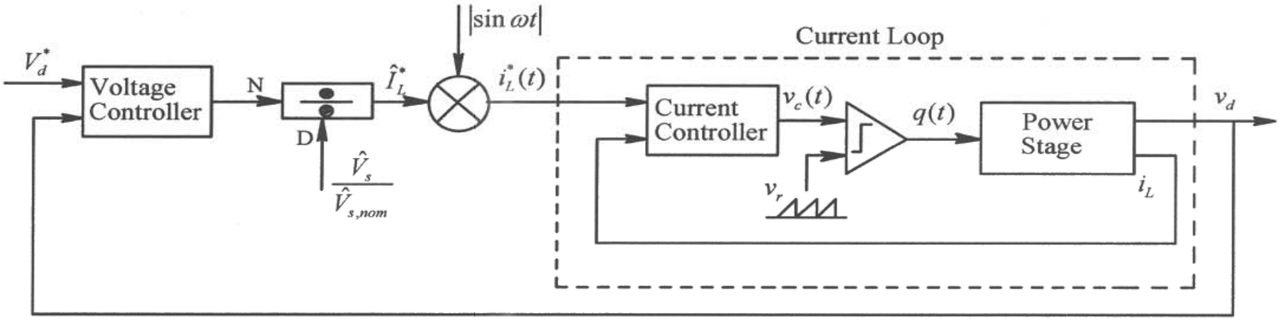


Figure 6-10 Feedforward of the input voltage.

REFERENCES

1. "UC3854 Controlled Power factor Correction Circuit Design," Philip C. Todd, Unitrode Application Note U-134.
2. "High power Factor Switching Pre-Regulator Design Optimization," Lyod Dixon, Unitrode Design Application Manual.
3. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.

PROBLEMS

6-1 In a single phase power factor correction circuit, $V_s = 120V(rms)$, $V_d = 225V$, and the output power is $100W$. Calculate and draw the following waveforms, synchronized to v_s waveform: $i_L(t)$, $d(t)$, and the current through the diode.

6-2 In the numerical example given in this chapter, calculate the rms input current if the utility voltage is $110V(rms)$, and compare it with its nominal value when $V_s = 120V(rms)$.

6-3 In problem 6-1, calculate the second-harmonic peak voltage in the capacitor if $C = 440\,\mu F$.

6-4 In the numerical example given in this chapter, calculate the maximum peak-peak ripple current in the inductor.

6-5 Repeat the design of the current loop in the given numerical example in this chapter, if the loop crossover frequency is $20\,kHz$.

6-6 Repeat the design of the outer voltage loop in the numerical example given in this chapter, if the output capacitance $C = 440\,\mu F$.

Chapter 7

MAGNETIC CIRCUIT CONCEPTS

The purpose of this chapter is to review some of the basic concepts associated with magnetic circuits and to develop an understanding of inductors and transformers, which are needed in power electronics.

7-1 AMPERE-TURNS AND FLUX

Let us consider a simple magnetic structure of Fig. 7-1 consisting of an N-turn coil with a current i, on a magnetic core made up of iron. This coil applies Ni ampere-turns to the core. We will assume the magnetic field intensity H_m in the core to be uniform along the mean path length ℓ_m. The magnetic field intensity in the air gap is denoted as H_g. From Ampere's Law, the closed line integral of the magnetic field intensity along the mean path within the core and in the air gap is equal to the applied ampere-turns:

$$H_m \ell_m + H_g \ell_g = Ni \tag{7-1}$$

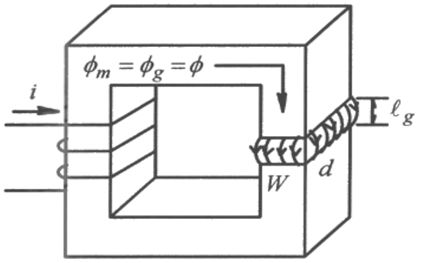


Figure 7-1 Magnetic structure with air gap.

In the core and in the air gap, the flux densities corresponding to H_m and H_g are as follows:

$$B_m = \mu_m H_m \tag{7-2}$$

$$B_g = \mu_o H_g \tag{7-3}$$

In terms of the above flux densities in Eq. 7-1,

$$\frac{B_m}{\mu_m} \ell_m + \frac{B_g}{\mu_o} \ell_g = Ni \tag{7-4}$$

Since flux lines form closed paths, the flux crossing any perpendicular cross-sectional area in the core is the same as that crossing the air gap. Therefore,

$$\phi = A_m B_m = A_g B_g \tag{7-5}$$

$$B_m = \frac{\phi}{A_m} \quad \text{and} \quad B_g = \frac{\phi}{A_g} \tag{7-6}$$

Substituting flux densities from Eq. 7-6 into Eq. 7-4,

$$\phi(\underbrace{\frac{\ell_m}{A_m \mu_m}}_{\Re_m} + \underbrace{\frac{\ell_g}{A_g \mu_o}}_{\Re_g}) = Ni \tag{7-7}$$

In Eq. 7-7, the two terms within the parenthesis equal the reluctance $\Re_m$ of the core and the reluctance $\Re_g$ of the air gap, respectively. Therefore, the effective reluctance $\Re$ of the whole structure in the path of the flux lines is the sum of the two reluctances:

$$\Re = \Re_m + \Re_g \tag{7-8}$$

Substituting from Eq. 7-8 into Eq. 7-7

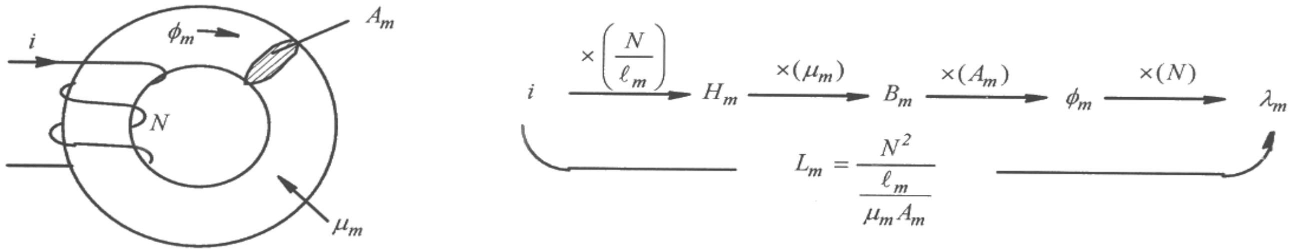
$$\phi = \frac{Ni}{\Re} \tag{7-9}$$

Eq. 7-9 allows the flux ϕ to be calculated for the applied ampere-turns, and hence B_m and B_g can be calculated from Eq. 7-6.

7-2 INDUCTANCE L

At any instant of time in the coil of Fig. 7-2a, the flux linkage of the coil λ_m, due to flux lines entirely in the core, is equal to the flux ϕ_m times the number of turns N that are linked. This flux linkage is related to the current i by a parameter defined as the inductance L_m:

$$\lambda_m = N\phi_m = L_m i \tag{7-10}$$



(a) (b)

Figure 7-2 Coil Inductance.

where the inductance $L_m (= \lambda_m / i)$ is constant if the core material is in its linear operating region. The coil inductance in the linear magnetic region can be calculated by multiplying all the factors shown in Fig. 7-2b, which are based on earlier equations:

$$L_m = \frac{\lambda_m}{i} = \frac{\underbrace{\underbrace{\underbrace{\underbrace{\left(\frac{Ni}{\ell_m}\right)}_{H_m}\mu_m}_{B_m} A_m}_{\phi_m} N}_{\lambda_m}}{i} = \frac{N^2}{\left(\frac{\ell_m}{\mu_m A_m}\right)} = \frac{N^2}{\Re_m} \qquad (7\text{-}11)$$

Eq. 7-11 indicates that the inductance L_m is strictly a property of the magnetic circuit (i.e., the core material, the geometry, and the number of turns), provided the operation is in the linear range of the magnetic material, where the slope of its *B-H* characteristic can be represented by a constant μ_m.

7-2-1 Energy Storage due to Magnetic Fields

Energy in an inductor is stored in its magnetic field. From the study of electric circuits, we know that at anytime, with a current i, the energy stored in the inductor is

$$W = \frac{1}{2} L_m i^2 \ [J] \qquad (7\text{-}12)$$

where [*J*], for Joules, is a unit of energy. Initially assuming a structure without an air gap, such as in Fig. 7-2a, we can express the energy storage in terms of flux density, by substituting into Eq. 7-12 the inductance from Eq. 7-11, and the current from the Ampere's Law in Eq. 7-1:

$$W_m = \frac{1}{2}\frac{N^2}{\frac{\ell_m}{\mu_m A_m}} \underbrace{(H_m \ell_m / N)^2}_{i^2} = \frac{1}{2}\frac{(H_m \ell_m)^2}{\frac{\ell_m}{\mu_m A_m}} = \frac{1}{2}\frac{B_m^2}{\mu_m}\underbrace{A_m \ell_m}_{volume} \quad [J] \qquad (7\text{-}13)$$

where $A_m \ell_m = volume$, and in the linear region $B_m = \mu_m H_m$. Therefore, from Eq. 7-13, the energy density in the core is

$$w_m = \frac{1}{2}\frac{B_m^2}{\mu_m} \qquad (7\text{-}14)$$

Similarly, the energy density in the air gap depends on μ_o and the flux density in it. Therefore, from Eq. 7-14, the energy density in any medium can be expressed as

$$w = \frac{1}{2}\frac{B^2}{\mu} \quad [J/m^3] \tag{7-15}$$

In inductors, the energy is primarily stored in the air gap purposely introduced in the path of flux lines.

In transformers, there is no air gap in the path of the flux lines. Therefore, the energy stored in the core of an ideal transformer is zero, where the core permeability is assumed infinite, and hence H_m is zero for a finite flux density. In a real transformer, the core permeability is finite, resulting in some energy storage in the core.

7-3 FARADAY'S LAW: INDUCED VOLTAGE IN A COIL DUE TO TIME-RATE OF CHANGE OF FLUX LINKAGE

In our discussion so far, we have established in magnetic circuits relationships between the electrical quantity i and the magnetic quantities H, B, ϕ, and λ. These relationships are valid under dc (static) conditions, as well as at any instant when these quantities are varying with time. We will now examine the voltage across the coil under time-*varying* conditions. In the coil of Fig. 7-3, Faraday's Law dictates that the time-rate of change of flux-linkage equals the voltage across the coil at any instant:

$$e(t) = \frac{d}{dt}\lambda(t) = N\frac{d}{dt}\phi(t) \tag{7-16}$$

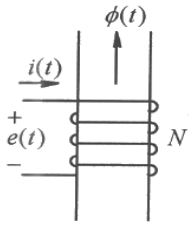


Figure 7-3 Voltage polarity and direction of flux and current.

This assumes that all flux lines link all *N*-turns such that $\lambda = N\phi$. The polarity of the emf $e(t)$ and the direction of $\phi(t)$ in the above equation are yet to be justified.

The relationship in Eq. 7-16 is valid, no matter what is causing the flux to change. One possibility is that a second coil is placed on the same core. When the second coil is supplied by a time-varying current, mutual coupling causes the flux ϕ through the coil to change with time. The other possibility is that a voltage $e(t)$ is applied across the coil in Fig. 7-3, causing the change in flux, which can be calculated by integrating both sides of Eq. 7-16 with respect to time:

$$\phi(t) = \phi(0) + \frac{1}{N}\int_0^t e(\tau)\cdot d\tau \qquad (7\text{-}17)$$

where $\phi(0)$ is the initial flux at $t = 0$ and τ is a variable of integration.

Recalling the Ohm's law, $v = Ri$, the current direction through a resistor is into the terminal at the positive polarity. This is the passive sign convention. Similarly, in the coil of Fig. 7-3, we can establish the voltage polarity and the flux direction in order to apply Faraday's law, given by Eqs. 7-16 and 7-17. If the flux direction is given, we can establish the voltage polarity as follows: first determine the direction of a hypothetical current that will produce flux in the same direction as given. Then, the positive polarity for the voltage is at the terminal, which this hypothetical current is entering. Conversely, if the voltage polarity is given, imagine a hypothetical current entering the positive-polarity terminal. This current, based on how the coil is wound, for example in Fig. 7-3, determines the flux direction for use in Eqs. 7-16 and 7-17. Following these rules to determine the voltage polarity and the flux direction is easier than applying Lenz's law (not discussed here).

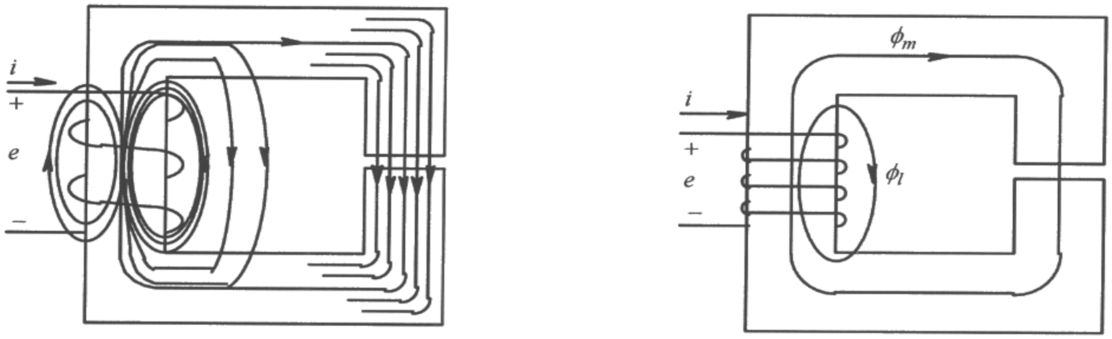
The voltage is induced due to $d\phi/dt$, regardless of whether any current flows in that coil.

7-4 LEAKAGE AND MAGNETIZING INDUCTANCES

Just as conductors guide currents in electric circuits, magnetic cores guide *flux* in *magnetic circuits*. But there is an important difference. In electric circuits, the conductivity of copper is approximately 10^{20} times higher than that of air, allowing leakage currents to be neglected at dc or at low frequencies such as 60 *Hz*. In magnetic circuits, however, the permeabilities of magnetic materials are, at best, only 10^4 times greater than that of air. Because of this relatively low ratio, the core window in the structure of Fig. 7-4a has "leakage" flux lines, which do not reach their intended destination that may be another winding, for example in a transformer, or an air gap in an inductor. Note that the coil shown in Fig. 7-4a is drawn schematically. In practice, the coil consists of multiple layers and the core is designed to fit as snugly to the coil as possible, thus minimizing the unused "window" area.

The leakage effect makes accurate analysis of magnetic circuits more difficult that requires sophisticated numerical methods, such as finite element analysis. However, we can account for the effect of leakage fluxes by making certain approximations. We can divide the total flux ϕ into two parts:

1. The magnetic flux ϕ_m, which is completely confined to the core and links all N turns, and
2. The leakage flux, which is partially or entirely in air and is represented by an "equivalent" leakage flux ϕ_ℓ, which also links all N turns of the coil but does not follow the entire magnetic path, as shown in Fig. 7-4b.



(a) (b)

Figure 7-4 (a) Magnetic and leakage fluxes; (b) equivalent representation of magnetic and leakage fluxes.

In Fig. 7-4b, $\phi = \phi_m + \phi_\ell$, where ϕ is the equivalent flux which links all N turns. Therefore, the total flux linkage of the coil is

$$\lambda = N\phi = \underbrace{N\phi_m}_{\lambda_m} + \underbrace{N\phi_\ell}_{\lambda_\ell} = \lambda_m + \lambda_\ell \tag{7-18}$$

The total inductance (called the self-inductance) can be obtained by dividing both sides of Eq. 7-18 by the current i:

$$\underbrace{\frac{\lambda}{i}}_{L_{self}} = \underbrace{\frac{\lambda_m}{i}}_{L_m} + \underbrace{\frac{\lambda_\ell}{i}}_{L_\ell} \tag{7-19}$$

$$\therefore \qquad L_{self} = L_m + L_\ell \tag{7-20}$$

where L_m is often called the *magnetizing inductance* due to ϕ_m in the magnetic core, and L_ℓ is called the *leakage inductance* due to the leakage flux ϕ_ℓ. From Eqs. 7-19 and 7-20, the total flux linkage of the coil in Eq. 7-18 can be written as

$$\lambda = (L_m + L_\ell)i \tag{7-21}$$

Hence, from Faraday's law in Eq. 7-16,

$$e(t) = \underbrace{L_m \frac{di}{dt}}_{e_m(t)} + L_\ell \frac{di}{dt} \tag{7-22}$$

This results in the electrical circuit of Fig. 7-5a. In Fig. 7-5b, the voltage drop due to the leakage inductance can be shown separately so that the voltage induced in the coil is solely due to the magnetizing flux. The coil resistance R can then be added in series to complete the representation of the coil.

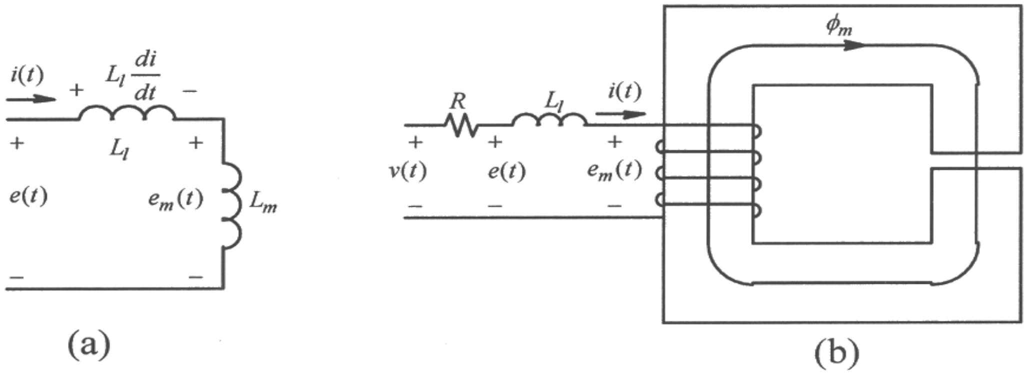


Figure 7-5 (a) Circuit representation;
(b) leakage inductance separated from the core.

7-4-1 Mutual Inductances

Most magnetic circuits, such as those encountered in inductors and transformers consist of multiple coils. In such circuits, the flux established by the current in one coil partially links the other coil or coils. This phenomenon can be described mathematically by means of mutual inductances, as examined in circuit theory courses. However, we will use simpler and more intuitive means to analyze mutually coupled coils, as in a Flyback converter discussed in Chapter 8 dealing with transformer-isolated dc-dc converters.

7-5 TRANSFORMERS

In power electronics, high-frequency transformers are essential to switch-mode dc power supplies. Such transformers often consist of two or more tightly coupled windings where almost all of the flux produced by one winding links the other windings. Including the leakage flux in detail makes the analysis very complicated and not very useful for our purposes here. Therefore, we will include only the magnetizing flux ϕ_m that links all the windings, ignoring the leakage flux whose consequences will be acknowledged separately.

To understand the operating principles of transformers, we will consider a three-winding transformer shown in Fig. 7-6 such that this analysis can be extended to any number of windings. In this transformer, all windings are linked by the same flux ϕ_m. Therefore, from the Faraday's law, the induced voltages at the dotted terminals with respect to their undotted terminals are as follows:

$$e_1 = N_1 \frac{d\phi_m}{dt} \tag{7-23}$$

$$e_2 = N_2 \frac{d\phi_m}{dt} \tag{7-24}$$

$$e_3 = N_3 \frac{d\phi_m}{dt} \tag{7-25}$$

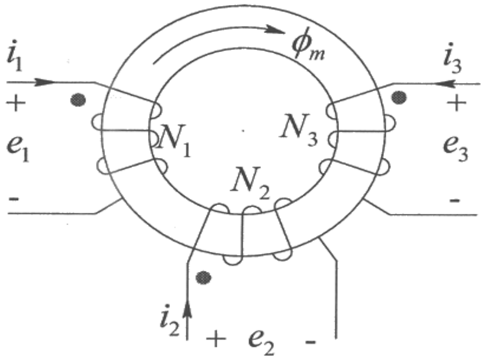


Figure 7-6 Transformer with three windings.

The above equations based on Faraday's law result in the following relationship that shows that the volts-per-turn induced in each winding are the same due to the same rate of change of flux that links them

$$\frac{d\phi_m}{dt} = \frac{e_1}{N_1} = \frac{e_2}{N_2} = \frac{e_3}{N_3} \tag{7-26}$$

In accordance to the Ampere's law given in Eq. 7-9, the flux ϕ_m at any instant of time is supported by the net ampere-turns applied to the core in Fig. 7-6,

$$\phi_m = \frac{N_1 i_1 + N_2 i_2 + N_3 i_3}{\Re_m} \tag{7-27}$$

In Eq. 7-27, the core of Fig. 7-6 offers reluctance $\Re_m$ in the flux path and the currents are defined positive into the dotted terminals of each winding such as to produce flux lines in the same direction. Eqs. 7-26 and 7-27 are the key to understanding transformers: at any instant of time, applied voltage (equal to the induced voltage if the winding resistance and the leakage flux are ignored) to one of the windings dictates the flux rate-of-change and hence the induced voltage-per-turn in other windings. The instantaneous flux ϕ_m is obtained by expressing Eq. 7-26 in its integral form below (with proper integral limits)

$$\phi_m = \frac{1}{N_1} \int e_1 dt = \frac{1}{N_2} \int e_2 dt = \frac{1}{N_3} \int e_3 dt \tag{7-28}$$

that requires corresponding net ampere-turns given by Eq. 7-27 to sustain this flux, overcoming the core reluctance. It is important to note that it is immaterial to the core the apportionment of these winding currents.

The analysis above is based on neglecting the leakage flux, assuming that the flux produced by a winding links all the other windings. In a simplified analysis, the leakage flux of a winding can be assumed to result in a leakage inductance, which can be added, along with the winding resistance, in series with the induced voltage $e(t)$ in the winding in the electrical circuit representation.

REFERENCE

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.

PROBLEMS

Inductors

A magnetic core has the following properties: the core area $A_m = 0.931 cm^2$, the magnetic path length of $\ell_m = 3.76 cm$, and the relative permeability of the material is $\mu_r = \mu_m / \mu_o = 5000$.

7-1 Calculate the reluctance $\Re$ of this core.

7-2 Calculate the reluctance of an air gap of length $\ell_g = 1 mm$, if it is introduced in the core of Problem 7-1.

7-3 A coil with $N = 30$ turns is wound on a core with an air gap described in Problem 7-2. Calculate the inductance of this coil.

7-4 If the flux density in the core in Problem 7-3 is not to exceed $0.2 T$, what is the maximum current that can be allowed to flow through this inductor coil?

7-5 At the maximum current calculated in Problem 7-4, calculate the energy stored in the magnetic core and the air gap, and compare the two.

Transformers

A three-winding transformer with $N_1 = 10$ turns, $N_2 = 5$ turns, and $N_3 = 5$ turns uses a magnetic core that has the following properties: $A_m = 0.639 cm^2$, the magnetic path length of $\ell_m = 3.12 cm$, and the relative permeability of the material $\mu_r = \mu_m / \mu_o = 5000$. A square-wave voltage, of 30-V amplitude and a frequency of 100 *kHz*, is applied to winding 1. Windings 2 and 3 are open. Ignore the leakage inductances.

7-6 Calculate and draw the magnetizing current waveform, along with the applied voltage waveform, and the waveforms of the voltages induced in the open windings 2 and 3.

7-7 Calculate the self-inductances of each winding in Problem 7-6.

7-8 Calculate the peak flux density in Problem 7-6.

7-9 A load resistance of 10Ω is connected to winding 2. Calculate and draw the currents in windings 1 and 2, along with the applied voltage waveform.

7-10 Assuming that winding 1 is not applied a voltage, what is the peak amplitude of the square-wave voltage at 100 *kHz* that can be applied to winding 3 of this transformer, if the peak flux density calculated in Problem 7-8 is not to be exceeded?

7-11 In Problem 7-6, what is the peak amplitude of the voltage that can be applied to winding 1 without exceeding the peak flux density calculated in Problem 7-8, if the frequency of the square wave voltage is 200kHz? What is the peak value of the magnetizing current, as compared to the one at 100 *kHz*?

Chapter 8

SWITCH-MODE DC POWER SUPPLIES

8-1 APPLICATIONS OF SWITCH-MODE DC POWER SUPPLIES

Switch-mode dc power supplies represent an important power electronics application area with the worldwide market in excess of several billion dollars per year. Many of these power supplies incorporate transformer isolation for reasons that are discussed below. Within these power supplies, transformer-isolated dc-dc converters are derived from non-isolated dc-dc converter topologies already discussed in chapter 3. For short, we will refer to transformer-isolated switch-mode dc power supplies as SMPS, whose block diagram is shown in Fig. 8-1. As shown in Fig. 8-1, these supplies encompass the rectification of the utility supply and the voltage V_{in} across a large filter capacitor is the input to the transformer-isolated dc-dc converter, which is the focus of discussion in this chapter. Internally, the transformer operates at very high frequencies, upwards of a few hundred kHz are typical, thus resulting in small size and weight, as discussed in the next chapter.

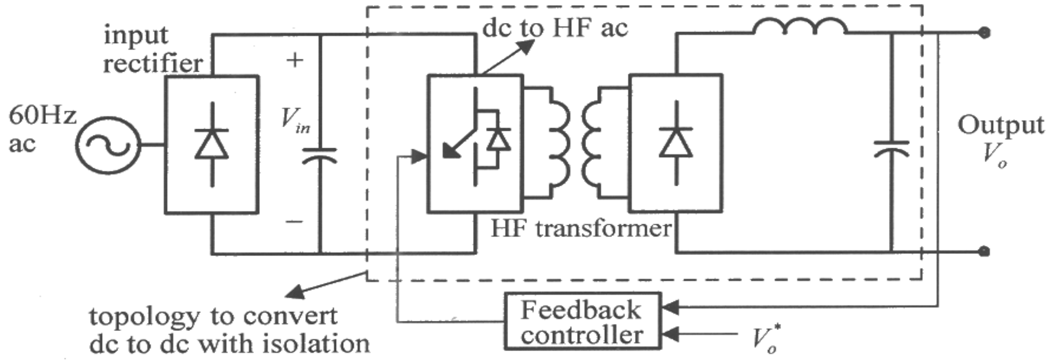


Figure 8-1 Block diagram of switch-mode dc power supplies.

8-2 NEED FOR ELECTRICAL ISOLATION

Electrical isolation by means of transformers is needed in switch-mode dc power supplies for three reasons:

1. Safety. It is necessary for the low-voltage dc output to be isolated from the utility supply to avoid the shock hazard.
2. Different Reference Potentials. The dc supply may have to operate at a different potential, for example, the dc supply to the gate drive for the upper MOSFET in the power-pole is referenced to its Source.

3. Voltage matching. If the dc-dc conversion is large, then to avoid requiring large voltage and current ratings of semiconductor devices, it may be economical and operationally more suitable to use an electrical transformer for conversion of voltage levels.

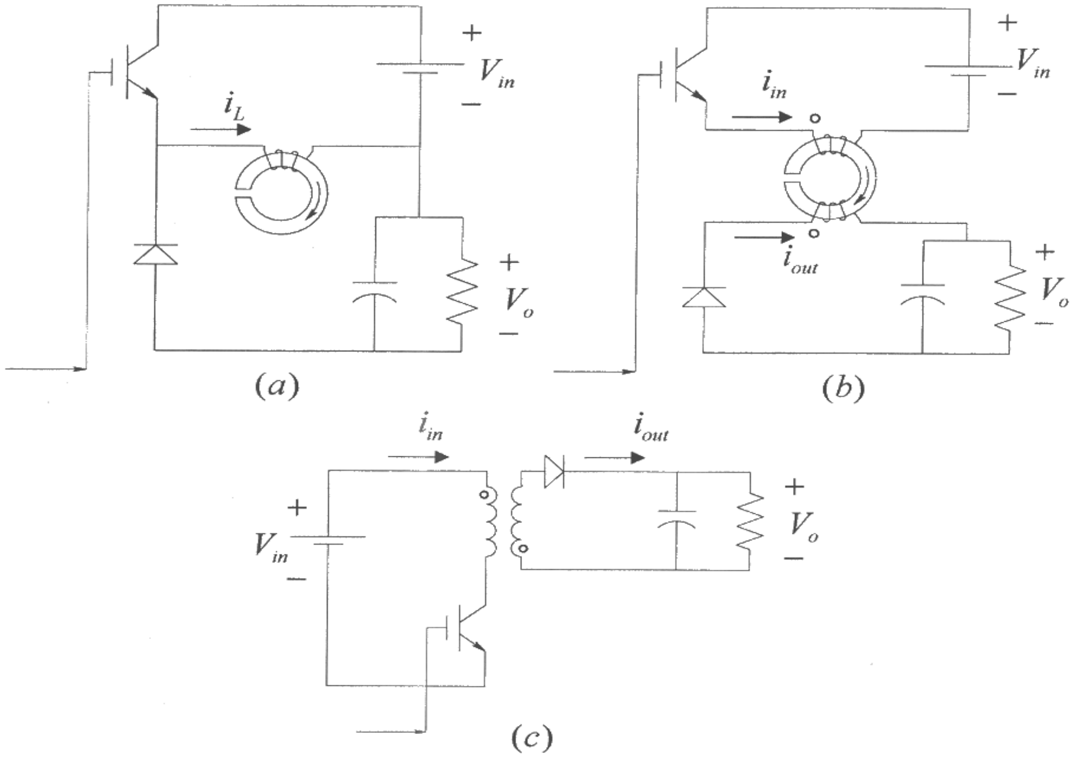
8-3 CLASSIFICATION OF TRANSFORMER-ISOLATED DC-DC CONVERTERS

In the block diagram of Fig. 8-1, there are following three categories of transformer-isolated dc-dc converters, all of which are discussed in detail in this chapter:

- Flyback converters derived from Buck-Boost dc-dc converters
- Forward converter derived from Buck dc-dc converters
- Full-Bridge and Half-Bridge converters derived from Buck dc-dc converters

8-4 FLYBACK CONVERTERS

Flyback converters are very commonly used in applications at low power levels below 50 W. These are derived from the Buck-Boost converter redrawn in Fig 8-2a, where the inductor is drawn descriptively on a low permeability core.



(a) (b)

(c)

Figure 8-2 Buck-Boost and the Flyback converters.

The Flyback converter in Fig. 8-2b consists of two mutually-coupled coils, where the coil orientations are such that at the instant when the transistor is turned-off, the current switches to the second coil to maintain the same flux in the core. Therefore, the dots on coils are as shown in Fig. 8-2b where the current into the dot of either coil produces core flux in the same direction. Commonly, the circuit of Fig. 8-2b is redrawn as in Fig. 8-2c.

We will consider the steady state in the incomplete demagnetization mode where the energy is never completely depleted from the magnetic core. This corresponds to the continuous conduction mode (CCM) in Buck-Boost converters. We will assume ideal devices and components, the output voltage $v_o(t) = V_o$, and the leakage inductances to be zero.

Turning on the transistor at $t = 0$ in the circuit in Fig. 8-2c applies the input voltage V_{in} across coil 1, and the core magnetizing flux ϕ_m increases linearly from its initial value $\phi_m(0)$, as shown in the waveforms of Fig. 8-3. During the transistor on-interval DT_s, the increase in flux can be calculated from the Faraday's law as

$$\Delta\phi_{p-p} = \frac{V_{in}}{N_1} DT_s \tag{8-1}$$

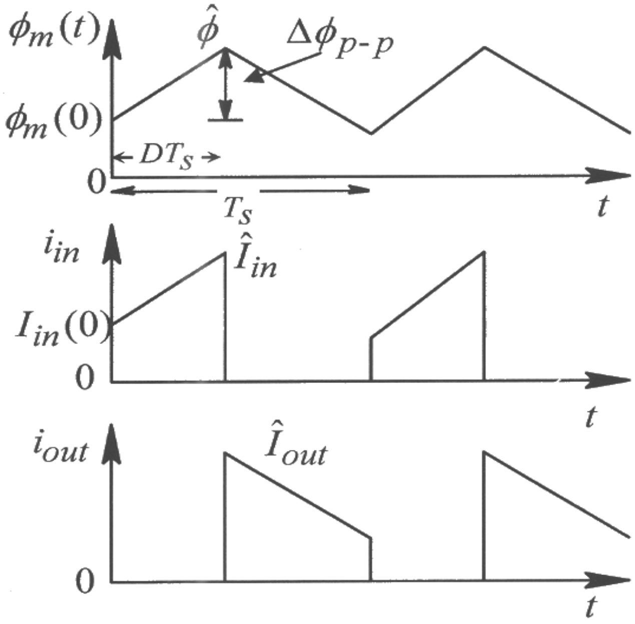


Figure 8-3 Flyback converter waveforms.

Due to increasing ϕ_m, the induced voltage $(N_2/N_1)V_{in}$ across coil 2 adds to the output voltage V_o to reverse bias the diode, resulting in $i_{out} = 0$. Corresponding to the core flux, the current i_{in} can be calculated using the relationship $\phi = Ni/\Re$, where $\Re$ is the core reluctance in the flux path. Therefore, using Eq. 8-1, the increase in the input current during the on-interval, from its initial value $I_{in}(0)$ can be calculated using Eq. 8-1 as

$$\Delta i_{in} = \frac{\Re}{N_1^2} V_{in} D T_s \tag{8-2}$$

During the on-interval DT_s, the output load is entirely supplied by the energy stored in the output capacitor, and the core magnetizing flux and the input current reach their peak values at the end of this interval:

$$\hat{\phi}_m = \phi_m(0) + \frac{V_{in}}{N_1} DT_s \tag{8-3}$$

$$\hat{I}_{in} = I_{in}(0) + \frac{\Re}{N_1^2} V_{in} DT_s \tag{8-4}$$

After the on-interval, turning off the transistor forces the input current in Fig. 8-2c to zero. The magnetic energy stored in the magnetic core due to the flux ϕ_m cannot change instantaneously, and hence the ampere-turns applied to the core must be the same at the instant immediately before and after turning the transistor off. Therefore, the current i_{out} in coil 2 through the diode suddenly jumps to its peak value such that

$$N_2 \hat{I}_{out}\Big|_{i_{in}=0} = N_1 \hat{I}_{in}\Big|_{i_{out}=0} \tag{8-5}$$

$$\therefore \quad \hat{I}_{out} = \frac{N_1}{N_2} \hat{I}_{in} \tag{8-6}$$

With the diode conducting, the output voltage V_o appears across coil 2 with a negative polarity. Hence, during the off-interval $(1-D)T_s$, the core flux declines linearly, as plotted in Fig. 8-3, by $\Delta\phi_{p-p}$, where

$$\Delta\phi_{p-p} = \frac{V_o}{N_2}(1-D)T_s \tag{8-7}$$

Using Eqs. 8-1 and 8-7,

$$\frac{V_o}{V_{in}} = \left(\frac{N_2}{N_1}\right)\frac{D}{1-D} \tag{8-8}$$

The change in the current $i_{out}(t)$ can be calculated in a manner similar to Eq. 8-2, and this current is plotted in Fig. 8-3.

Eq. 8-8 shows that in a Flyback converter, the dependence of the voltage-ratio on the duty-ratio D is identical to that in the Buck-Boost converter, and it also depends on the coils turns-ratio N_2 / N_1. Flyback converters require minimum number of components by integrating the inductor (needed for a Buck-Boost operation) with the transformer that provides electrical isolation and matching of the voltage levels. These converters are very commonly used in low power applications in the complete demagnetization mode (corresponding to the discontinuous-conduction mode in Buck-Boost), which makes their control easier. A disadvantage of the Flyback converter is the need for snubbers to prevent voltage spikes across the transistor and diode due to leakage inductances associated with the two coils.

8-5 FORWARD CONVERTERS

Forward converter and its variations derived from a Buck converter are commonly used in applications at low power levels up to a kW. A Buck converter is shown in Fig. 8-4a. In this circuit, a three-winding transformer is added as shown in Fig. 8-4b to realize a Forward converter. The third winding in series with a diode D_3, and the diode D_1 are needed to demagnetize the core every switching cycle. The winding orientations in Fig. 8-4b are such that the current into the dot of any of the windings will produce core flux in the same direction. We will consider steady state converter operation in the continuous conduction mode where the output inductor current i_L flows continuously. In the following analysis, we will assume ideal semiconductor devices, $v_o(t) = V_o$, and the leakage inductances to be zero.

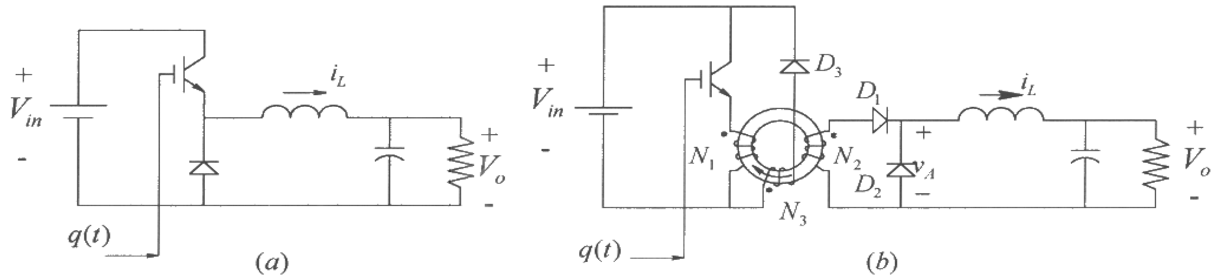


Figure 8-4 Buck and Forward converters.

Initially, assuming an ideal transformer in the Forward converter of Fig. 8-4b, the third winding and the diode D_3 can be removed and D_1 can be replaced by a short circuit. In such an ideal case, the Forward converter operation is identical to that of the Buck converter, as shown by the waveform in Fig. 8-5, except for the presence of the transformer turns-ratio N_2 / N_1. Therefore, in the continuous conduction mode,

$$V_o = \left(\frac{N_2}{N_1} \right) D V_{in} \tag{8-9}$$

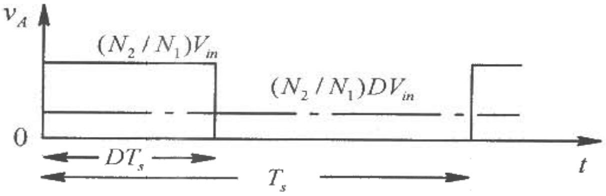


Figure 8-5 Forward converter operation.

In the case with a real transformer, the core must be completely demagnetized during the off-interval of the transistor, and hence the need for the third winding and the diodes D_1 and D_3, as shown in Fig. 8-4b. Turning on the transistor causes the magnetizing flux in the core to build up as shown in Fig. 8-6. During this on-interval DT_s, D_3 gets reverse biased, thus preventing the current from flowing through the tertiary winding. The diode D_2 also gets reversed biased and the output inductor current flows through D_1.

When the transistor is turned off, the magnetic energy stored in the transformer core forces a current to flow into the dotted terminal of the tertiary winding, since the current into the dotted terminal of the secondary winding cannot flow due to D_1, which results in V_{in} to be applied negatively across the tertiary winding, and the core flux to decline, as shown in Fig. 8-6. (The output inductor current freewheels through D_2.) After an interval T_{demag}, the core flux comes to zero and stays zero during the remaining interval, until the next cycle begins.

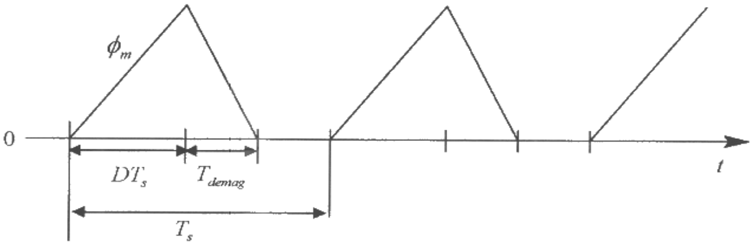


Fig. 8-6 Forward converter core flux.

To avoid the core from saturating, T_{demag} must be less than the off-interval $(1-D)T_s$ of the transistor. Typically, windings 1 and 3 are wound bifilar to provide a very tight mutual coupling between the two, and hence, $N_3 = N_1$. Therefore, to the core is applied an equal magnitude but opposite polarity per-turn voltage during DT_s and T_{demag}, respectively. At the upper limit, T_{demag} equals $(1-D)T_s$, and equating it to the on-interval DT_s of the transistor yields the upper limit on the duty-ratio, $D_{\max}$, to be 0.5, with $N_1 = N_3$.

8-5-1 Two-Switch Forward Converters

Single-switch Forward converters are used in power ratings up to a few hundred watts. However, Two-Switch Forward converters discussed below eliminate the need for a separate demagnetizing winding and are used in much higher power ratings of a kW and even higher.

Fig. 8-7 shows the topology of the Two-Switch Forward converter, where both transistors are gated on and off simultaneously with a duty-ratio $D \le 0.5$. During the on-interval DT_s when both transistors are on, diodes D_1 and D_2 get reverse biased and the output inductor current i_L flows through D_o, similar to that in a single-switch Forward converter. During the off interval when both transistors are turned off, the magnetizing current in the transformer core flows through the two primary-side diodes into V_{in}, thus applying V_{in} negatively to the core and causing it to demagnetize. Application of $-V_{in}$ to the primary winding causes D_o to get reversed biased and the output inductor current i_L freewheels through D_F.

Based on the discussion regarding the demagnetization of the core in a single-switch Forward converter, the switch duty-ratio D is limited to 0.5. The voltage conversion ratio remains the same as in Eq. 8-9.

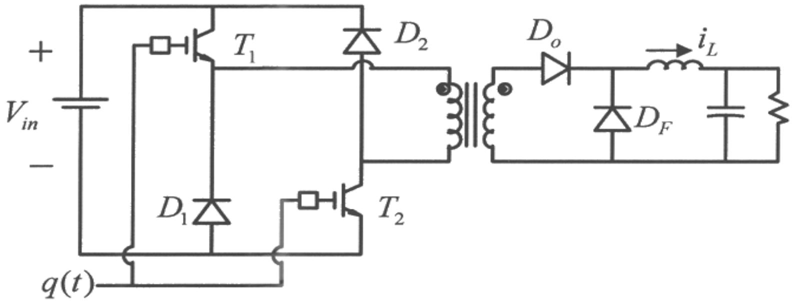


Figure 8-7 Two-switch Forward converter.

8-6 FULL-BRIDGE CONVERTERS

Full-Bridge converters consist of four transistors, hence are economically feasible only at higher power levels in applications at a few hundred watts and higher. Like Forward converters, full-bridge converters are also derived from Buck converters. Unlike Flyback and Forward converters that operate in only one quadrant of the B-H loop, Full-Bridge converters use the magnetic core in two quadrants.

A Full-Bridge converter consists of two switching power-poles, as shown in Fig. 8-8, with a center-tapped transformer secondary winding. In analyzing this converter, we will assume the transformer ideal, although the effects of magnetizing current can be easily accounted for. We will consider steady state converter operation in the continuous conduction mode where the output inductor current i_L flows continuously. As with previous converters, we will assume ideal devices and components, and $v_o(t) = V_o$.

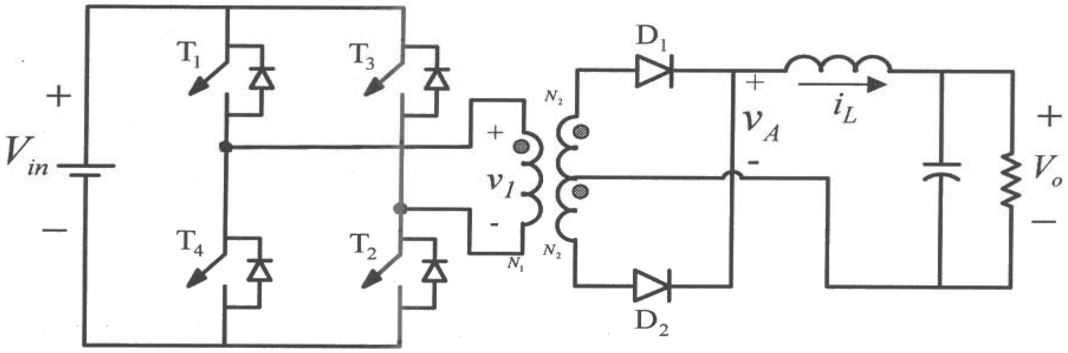


Figure 8-8 Full-Bridge converter.

In the Full-Bridge converter of Fig. 8-8, the voltage v_1 applied to the primary winding alternates without a dc component. The waveform of this voltage is shown in Fig. 8-9, where $v_1 = V_{in}$ when transistors T_1 and T_2 are on during DT_s, and $v_1 = -V_{in}$ when T_3 and T_4 are on for an interval of the same duration. This waveform applies equal positive and negative volt-seconds to the transformer primary. The switch duty-ratio D (< 0.5) is controlled to achieve the output voltage regulation by means of zero intervals between the positive and the negative applied voltages.

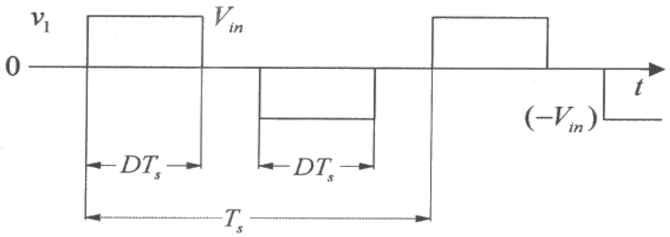


Figure 8-9 Full-Bridge converter waveforms.

The way the voltage across the primary winding, hence the secondary winding, is forced to be zero classifies Full-Bridge converters into the following two categories:

- Pulse-Width Modulated (PWM), and
- Phase-Shift Modulated (PSM)

PWM Control. In PWM control, all four transistors are turned off, resulting in a zero voltage across the transformer windings, as discussed shortly. With all transistors off, the output inductor current freewheels through the two secondary windings, and there are no conduction losses on the primary side of the transformer. Therefore, the PWM control results in lower conduction losses, and it is the control method discussed in this chapter.

PSM Control. In phase-shift modulated control, the two transistors of each power-pole are operated at nearly 50% duty-ratio, with $D \simeq 0.5$. The output of each power-pole pulsates between V_{in} and 0 with a duty-ratio of nearly 50%. The length of the zero intervals is controlled by phase-shifting the two power-pole outputs with respect to each other, as the name of this control implies. During zero intervals, either both transistors at the top, or both transistors at the bottom are on, creating a short circuit (through one of the anti-parallel diodes, depending on the direction of the current) across the primary winding, resulting in $v_1 = 0$. During this short-circuited condition, the output inductor current is reflected to the primary winding and circulates through the primary-side semiconductor devices, causing additional conduction losses. However, increased conduction losses can be offset by the reduction in switching losses by this means of control, as we will discuss in detail in Chapter 10 on soft-switching.

8-6-1 PWM Control

As shown by the block diagram of Fig. 8-10a, the PWM-IC for Full-Bridge converters provides gate signals to the transistor pairs (T_1, T_2 and T_3, T_4) during alternate cycles of the ramp voltage in Fig. 8-10b.

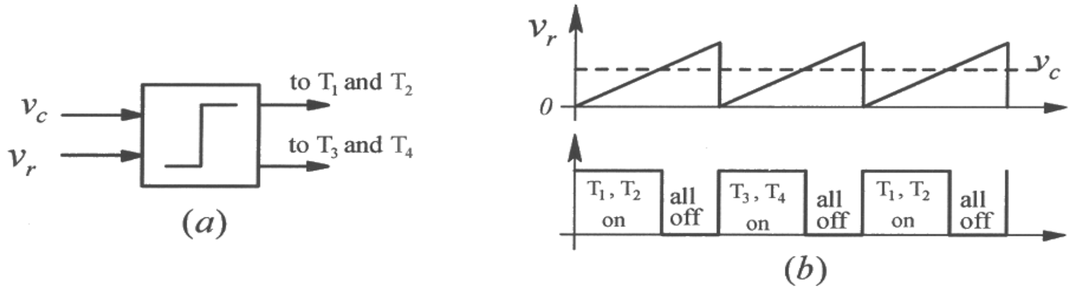


Figure 8-10 PWM-IC and control signals for transistors.

Corresponding to these PWM switching signals, the resulting sub-circuits are shown in Fig. 8-11 for one-half switching cycle, where the other half-cycle is symmetric.

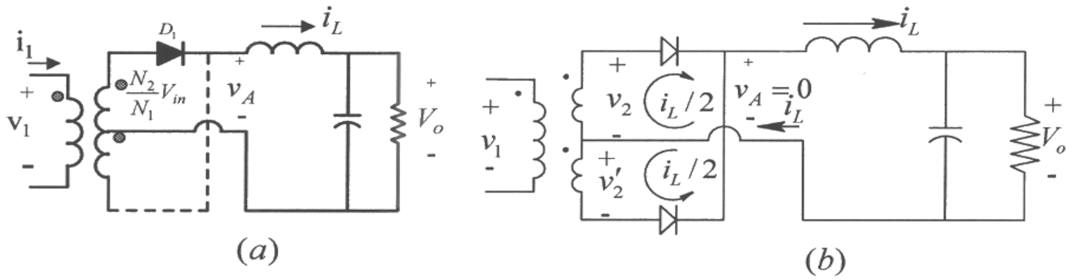


Figure 8-11 Full-Bridge: sub-circuits.

Interval DT_s with transistors T_1, T_2 in their on state. Turning on T_1, T_2 applies positive voltage V_{in} to the primary winding, causing D_2 to become reverse biased and i_L is carried through D_1, as shown in Fig. 8-11a. During this interval, $v_A = (N_2 / N_1) V_{in}$ as plotted in Fig. 8-12.

Interval $(1/2 - D)T_s$ with all Transistors off. When all the transistors are turned off, there is no current in the primary winding, and the output inductor current divides equally (assuming an ideal transformer) between the two output diodes as shown in the sub-circuit of Fig. 8-11b. This ensures that the total ampere-turns acting on the transformer core equal zero because of $i_L / 2$ coming out of the dotted terminal and $i_L / 2$ going into the dotted terminal. Applying the Kirchhoff's voltage law in the loop consisting of the two secondaries in Fig. 8-11b shows that $v_2 + v_2' = 0$. Since $v_2 = v_2'$, the two voltages must be individually zero, and hence also the primary voltage v_1:

$$v_1 = v_2 = v_2' = 0 \tag{8-10}$$

During this interval, $v_A = 0$ as plotted in Fig. 8-12.

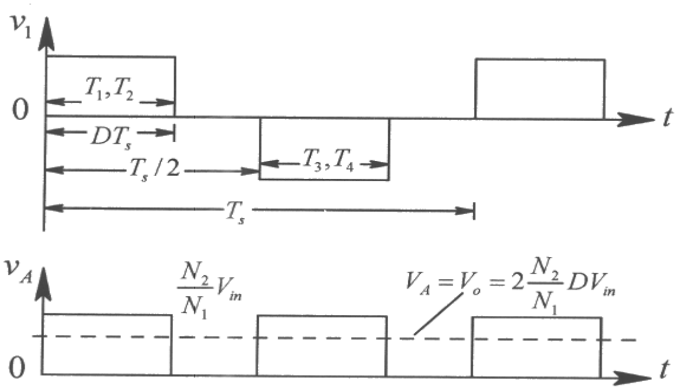


Figure 8-12 Full-Bridge converter waveforms.

The above discussion completes the discussion of one-half switching cycle. The other half-cycle with T_3, T_4 on applies a negative voltage ($-V_{in}$) across the primary winding for an interval DT_s and results in D_2 conducting and D_1 reverse biased. During this interval, $v_A = (N_2 / N_1) V_{in}$ as before when the positive voltage was applied to the primary winding. The waveforms during this half-cycle are as plotted in Fig. 8-12.

From Fig. 8-12, recognizing that $V_A = V_o$ in the dc steady state,

$$\frac{V_o}{V_{in}} = 2\left(\frac{N_2}{N_1}\right) D \tag{8-11}$$

8-7 Half-Bridge and Push-Pull Converters

Variations of Full-Bridge converters are shown in Fig. 8-13. The Half-Bridge converter in Fig. 8-13a consists of only two transistors but requires two split capacitors to form a dc input mid-point. It is sometimes used at slightly lower power levels compared to the Full-Bridge converter. The Push-Pull converter in Fig. 8-13b has the advantage of having both transistors gates referenced to the low-side of the input voltage. The penalty is in the transformer where during the power transfer interval, only one half of the primary winding and one half of the secondary winding are utilized.

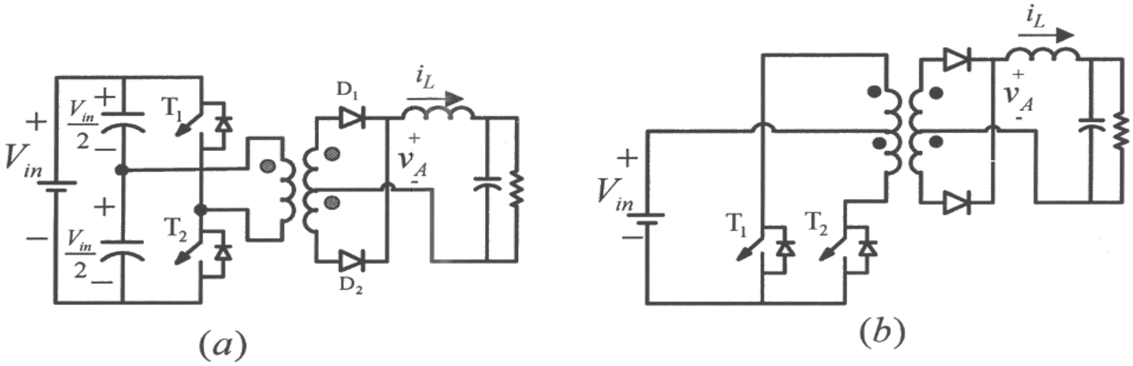


Figure 8-13 Half-Bridge and Push-Pull converters.

8-8 PRACTICAL CONSIDERATIONS

To provide electrical isolation between the input and the output, the feedback control loop should also have electrical isolation. There are several ways of providing this isolation as discussed in Reference [1].

REFERENCE

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.

PROBLEMS

Flyback Converters:

In a Flyback converter, $V_{in} = 30V$, $N_1 = 30$ turns, and $N_2 = 15$ turns. The self-inductance of winding 1 is $50\,\mu H$, and $f_s = 200\,kHz$. The output voltage is regulated at $V_o = 9V$.

8-1 Calculate and draw the waveforms shown in Fig 8-3 along with the ripple current in the output capacitor, if the load is $27W$.

8-2 For the same duty-ratio as in Problem 8-1, calculate the critical power which makes this converter operate at the border of incomplete and complete demagnetization modes.

8-3 Draw the waveforms, similar to those in Problem 8-1, in Problem 8-2.

8-4 If a Flyback converter is operating in a complete de-magnetization mode, derive the voltage transfer ratio in terms of the load resistance R, the switching frequency f_s, the self-inductance L_1 of winding 1, and the duty-ratio D.

Forward converter:

In a Forward converter, $V_{in} = 30V$, $N_1 = 10$ turns, $N_2 = 5$ turns, and $N_3 = 10$ turns. The self-inductance of winding 1 is $150\,\mu H$, and the switching frequency $f_s = 200\,kHz$. The output voltage is regulated such that $V_o = 5V$. The output filter inductance is $50\,\mu H$, and the output load is $25W$.

8-5 Calculate and draw the waveforms for v_A, i_L, i_{in}, and i_{D_3} in Fig. 8-4b.

8-6 If the maximum duty ratio needs to be increased to 0.7, calculate N_1 / N_3?

8-7 Why is diode D_1 necessary in Fig 8-4b?

Two-Switch Forward Converters

In a two-switch Forward converter, $V_{in} = 30V$, $N_1 / N_2 = 2$, and the switching frequency $f_s = 200\,kHz$. The output voltage is regulated such that $V_o = 5V$. The self-inductance of winding 1 is $150\,\mu H$, and the output filter inductance is $50\,\mu H$.

8-8 Calculate and draw waveforms if the output load is $200W$.

8-9 Why is the duty-ratio in this converter limited to 0.5?

Full-Bridge Converters

8-10 In a Full-bridge converter shown in Fig. 8-8, consider the output current through the filter inductor to be ripple-free dc. $V_{in} = 30V$, $f_s = 200\,kHz$, and $N_1 / N_2 = 4$. The output voltage is regulated such that $V_o = 5V$. Calculate the PWM waveforms in this converter. Assume the transformer ideal.

Chapter 9

Design of High-Frequency Inductors and Transformers

9-1 INTRODUCTION

As discussed Chapter 8, inductors and transformers are needed in switch-mode dc power supplies, where switching frequencies are in excess of 100 kHz. High-frequency inductors and transformers are generally not available off-the-shelf, and must be designed based on the application specifications. A detailed design discussion is presented in Reference [1]. In this chapter, a simple and a commonly used approach called the Area-Product method is presented, where the thermal considerations are ignored. This implies that the magnetic component built on the design basis presented here should be evaluated for its temperature rise and efficiency, and the core and the conductor sizes should be adjusted accordingly.

9-2 BASICS OF MAGNETIC DESIGN

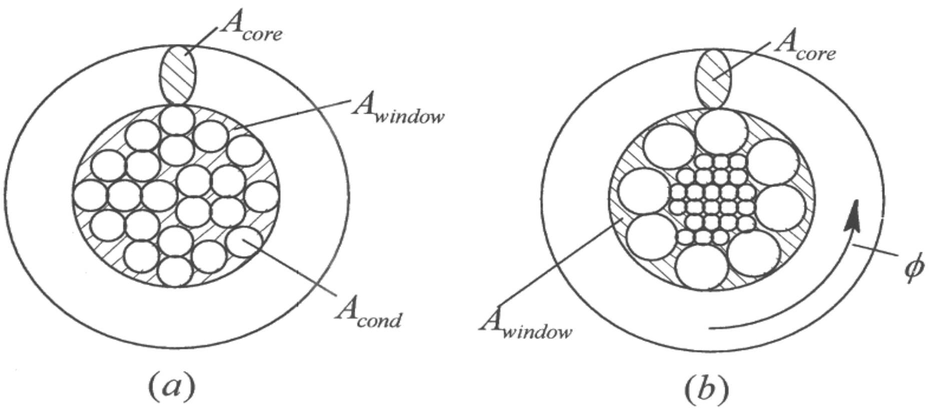
In designing high frequency inductors and transformers, a designer is faced with countless choices. These include choice of core materials, core shapes (some offer better thermal conduction whereas others offer better shielding to stray flux), cooling methods (natural convection versus forced cooling), and losses (lower losses offer higher efficiency at the expense of higher size and weight) to name a few. However, all magnetic design-optimization programs calculate two basic quantities from given electrical specifications:

- The peak flux density $B_{\max}$ in the magnetic core to limit core losses, and
- The peak current density $J_{\max}$ in the winding conductors to limit conduction losses

The design procedure presented in this chapter assumes values for these two quantities based on the intended applications of inductors and transformers. However, they may be far from optimum in certain situations.

9-3 INDUCTOR AND TRANSFORMER CONSTRUCTION

Figs. 9-1a and b represent the cross-section of an inductor and a transformer wound on toroidal cores. In Fig. 9-1a for an inductor, the same current i passes through all N turns of a winding. In the transformer of Fig. 9-1b, there are two windings where the current i_1 in winding 1, with N_1 bigger cross-section conductors, is in opposite direction to that of i_2 in winding 2 with N_2 smaller cross-section conductors. In each winding, the conductor cross-section is chosen such that the peak current density $J_{\max}$ is not exceeded at the maximum specified current in that winding. The core area A_{core} in Figs. 9-1a and b allows the flow of flux lines without exceeding the maximum flux density $B_{\max}$ in the core.



(a) (b)

Figure 9-1 Cross-sections.

9-4 AREA-PRODUCT METHOD

The area-product method, based on pre-selected values of the peak flux density $B_{\max}$ in the core and the peak current density $J_{\max}$ in the conductors, allows an appropriate core size to be chosen, as described below.

9-4-1 Core Window Area A_{window}

The windows of the toroidal cores in Figs. 9-1a and b accommodate the winding conductors, where the conductor cross-sectional area A_{cond} depends on the maximum rms current for which the winding is designed. In the expression for the window area below, the window fill-factor k_w in a range from 0.3 to 0.6 accounts for the fact that the entire area of the window cannot be filled, and the subscript y designates a winding, where in general there may be more than one, like in a transformer

$$A_{window} = \frac{1}{k_w} \sum_y \left(N_y A_{cond,y} \right) \tag{9-1}$$

In Eq. 9-1, the conductor cross-sectional area in winding y depends on its maximum rms current and the maximum allowed current density $J_{\max}$ that is generally chosen to be the same for all windings:

$$A_{cond,y} = \frac{I_{rms,y}}{J_{\max}} \tag{9-2}$$

Substituting Eq. 9-2 into Eq. 9-1,

$$A_{window} = \frac{\sum_{y} \left(N_y I_{rms,y} \right)}{k_w J_{\max}} \tag{9-3}$$

which shows that the window area is linearly proportional to the number of turns chosen by the designer.

9-4-2 Core Cross-Sectional Area A_{core}

The core cross-sectional area in Figs. 9-1a and b depends on the peak flux $\hat{\phi}$ and the choice of the maximum allowed flux density $B_{\max}$ to limit core losses:

$$A_{core} = \frac{\hat{\phi}}{B_{\max}} \tag{9-4}$$

How the flux is produced depends if the device is an inductor or a transformer. In an inductor, $\hat{\phi}$ depends on the peak current, where $L\hat{I}$ equals the peak flux linkage $N\hat{\phi}$. Hence,

$$\hat{\phi} = \frac{L\hat{I}}{N} \qquad \text{(inductor)} \tag{9-5}$$

In a transformer, based on the Faraday's law, the flux depends linearly on the applied volt-seconds and inversely on the number of turns. This is shown in Fig. 9-2 for a Forward converter transformer with $N_1 = N_3$, and the duty-ratio D, which is limited to 0.5. Therefore, we can express the peak flux in Fig. 9-2 as

$$\hat{\phi} = \frac{k_{conv} V_{in}}{N_1 f_s} \tag{9-6}$$

where the factor k_{conv} equals D in Forward converter, and typically has a maximum value of 0.5. The factor k_{conv} can be derived for transformers in other converter topologies based on the specified operating conditions, for example, it equals $D/2$ in a Full-Bridge converter. In general, the peak flux can be expressed in terms of any one of the windings, y for example, as

$$\hat{\phi} = \frac{k_{conv} V_y}{N_y f_s} \qquad \text{(transformer)} \tag{9-7}$$

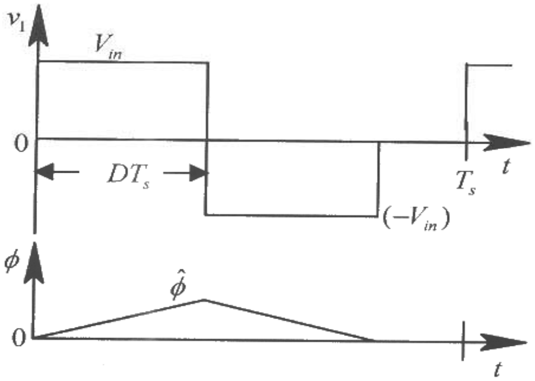


Figure 9-2 Waveforms in a transformer for a Forward converter.

Substituting for $\hat{\phi}$ from Eq. 9-5 or 9-7 into Eq. 9-4,

$$A_{core} = \frac{L\hat{I}}{NB_{\max}} \qquad (\text{inductor}) \qquad (9\text{-}8)$$

$$A_{core} = \frac{k_{conv}V_y}{N_y f_s B_{\max}} \qquad (\text{transformer}) \qquad (9\text{-}9)$$

Eqs. 9-8 and 9-9 show that in both cases, the core cross-sectional area is inversely proportional to the number of turns chosen by the designer.

9-4-3 Core Area-Product $A_p (= A_{core} A_{window})$

The core area-product is obtained by multiplying the core cross-sectional area A_{core} with its window area A_{window} :

$$A_p = A_{core} A_{window} \qquad (9\text{-}10)$$

Substituting for A_{window} and A_{core} from the previous equations,

$$A_p = \frac{L\hat{I}I_{rms}}{k_w J_{\max} B_{\max}} \qquad (\text{inductor}) \qquad (9\text{-}11)$$

$$A_p = \frac{k_{conv}\sum V_y I_{y,rms}}{k_w B_{\max} J_{\max} f_s} \qquad (\text{transformer}) \qquad (9\text{-}12)$$

Eqs. 9-11 and 9-12 show that the area-product that represents the overall size of the device is independent (as it ought to be) of the number of turns. After all, the core and the overall component size should depend on the electrical specifications and the assumed values of $B_{\max}$ and $J_{\max}$, and *not* on the number of turns which is an internal design variable.

9-4-4 Design Procedure Based on Area-Product A_p

Once we pick the appropriate material and the shape for a core, the cores by various manufacturers are cataloged based on the area-product A_p. Having calculated the value of A_p above, we can select the appropriate core. It should be noted that there are infinite combinations of the core cross-sectional area A_{core} and the window area A_{window} that yield a desired area-product A_p. However, manufacturers take pains in producing cores such that for a given A_p, a core has A_{core} and A_{window} that are individually optimized for power density. Once we select a core, it has specific A_{core} and A_{window}, which allow the number of turns to be calculated as follows:

$$N = \frac{L\hat{I}}{B_{\max} A_{core}} \qquad \text{(inductor ; from Eq. 9-8)} \qquad (9\text{-}13)$$

$$N_y = \frac{k_{conv} V_y}{A_{core} f_s B_{\max}} \qquad \text{(transformer ; from Eq. 9-9)} \qquad (9\text{-}14)$$

In an inductor, to ensure that it has the specified inductance, an air gap of an appropriate length ℓ_g is introduced in the path of flux lines. Assuming the chosen core material to have very high permeability, the core inductance is primarily dictated by the reluctance $\Re_g$ of the air gap, such that

$$L \simeq \frac{N^2}{\Re_g} \qquad (9\text{-}15)$$

where,

$$\Re_g \simeq \frac{\ell_g}{\mu_o A_{core}} \qquad (9\text{-}16)$$

Using Eqs. 9-15 and 9-16, the air gap length ℓ_g can be calculated as

$$\ell_g = \frac{N^2 \mu_o A_{core}}{L} \qquad (9\text{-}17)$$

The above equations are approximate because they ignore the effects of finite core permeability and the fringing flux, which can be substantial. Core manufacturers generally specify measured inductance as a function of the number of turn for various values of the air gap length. In this section, we used a toroidal core for descriptive purposes in which it will be difficult to introduce an air gap. If a toroidal core must be used, it can be picked with a distributed air gap such that it has the effective air gap length as calculated above. The above procedure explained for toroidal cores is equally valid for other types of cores. The actual design described in the next section illustrates the introduction of air gap in a pot core.

9-5 DESIGN EXAMPLE OF AN INDUCTOR

In this example, we will discuss the design of an inductor that has an inductance $L = 100\mu H$. The worst-case current through the inductor is shown in Fig. 9-3, where the average current $I = 5.0A$, and the peak-peak ripple $\Delta I = 0.75A$ at the switching frequency $f_s = 100kHz$. We will assume the following maximum values for the flux density and the current density: $B_{\max} = 0.25T$, and $J_{\max} = 6.0A/mm^2$ (for larger cores, this is typically in a range of 3 to $4A/mm^2$). The window fill factor is assumed to be $k_w = 0.5$.

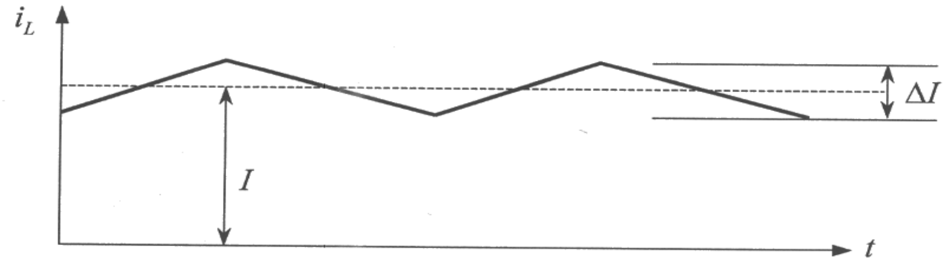


Figure 9-3 Inductor current waveforms.

The peak value of the inductor current from Fig. 9-3 is $\hat{I} = I + \frac{\Delta I}{2} = 5.375A$. The rms value of the current for the waveform shown in Fig. 9-3 can be calculated as $I_{rms} = \sqrt{I^2 + \frac{1}{12}\Delta I^2} \simeq 5.0A$ (the derivation is left as a homework problem).

From Eq. 9-11,

$$\text{Area-Product } A_p = \frac{100 \times 10^{-6} \times 5.375 \times 5}{0.5 \times 0.25 \times 6 \times 10^6} \times 10^{12} = 3587\, mm^4$$

From the Magnetics, Inc. catalog [2], we will select a P-type material, which has the saturation flux density of $0.5T$ and is quite suitable for use at the switching frequency of $100kHz$. A pot core 26×16, which is shown in Fig. 9-4 for a laboratory experiment, has the core Area $A_{core} = 93.1mm^2$ and the window Area $A_{window} = 39mm^2$. Therefore, we will select this core, which has an Area-Product $A_p = 93.1 \times 39 = 3631mm^4$. From Eq. 9-13,

$$N = \frac{100\mu \times 5.375}{0.25 \times 93.1 \times 10^{-6}} \simeq 23 \text{ Turns}$$

Winding wire cross sectional area $A_{cond} = I_{rms} / J_{\max} = 5.0/6.0 = 0.83 mm^2$. We will use five strands of American Wire Gauge AWG 25 wires [3], each with a cross-sectional area of $0.16 mm^2$, in parallel. From Eq. 9-17, the air gap length can be calculated as

$$\ell_g = \frac{23^2 \times 4\pi \times 10^{-7} \times 93.1 \times 10^{-6}}{100\mu} \simeq 0.62 mm .$$

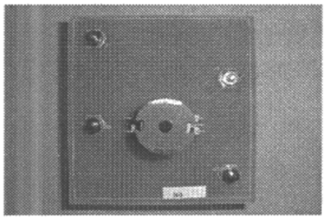


Figure 9-4 Pot core mounted on a plug-in board.

9-6 DESIGN EXAMPLE OF A TRANSFORMER FOR A FORWARD CONVERTER

The required electrical specifications for the transformer in a Forward converter are as follows: $f_s = 100kHz$ and $V_1 = V_2 = V_3 = 30V$. Assume the rms value of the current in each winding to be $2.5A$. We will choose the following values for this design: $B_{\max} = 0.25\text{T}$ and $J_{\max} = 5\,\text{A/mm}^2$. From Eq. 9-12, where $k_w = 0.5$ and $k_{conv} = 0.5$,

$$A_p = \frac{k_{conv}}{k_w f_s B_{\max} J_{\max}} \sum_y \hat{V}_y I_{rms,y} = 1800 \text{ mm}^4$$

For the pot core 22×13 [2], $A_{core} = 63.9 \text{ mm}^2$, $A_{window} = 29.2 \text{ mm}^2$, and therefore $A_p = 1866 \text{ mm}^4$. For this core, the winding wire cross-sectional area is obtained as

$$A_{cond,1} = \frac{I_{1,rms}}{J_{\max}} = \frac{2.5}{5} = 0.5 \text{ mm}^2 .$$

We will use three strands of AWG 25 wires [3], each with a cross-sectional area of $0.16 mm^2$, in parallel for each winding. From Eq. 9-14,

$$N_1 = \frac{0.5 \times 30}{\left(63.9 \times 10^{-6}\right) \times \left(100 \times 10^3\right) \times 0.25} \simeq 10 .$$

Hence,

$$N_1 = N_2 = N_3 = 10 .$$

9-7 THERMAL CONSIDERATIONS

Designs presented here do not include eddy current losses in the windings, which can be very substantial due to proximity effects in inductors. These effects are carefully considered in [1]. Therefore, the area-product method is a good starting point, but the designs must be evaluated for temperature rise based on thermal considerations.

REFERENCES

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.
2. Magnetics, Inc. Ferrite Cores (www.mag-inc.com).
3. Wire Gauge Comparison Chart (www.tool-portals.com/de/umrechnung/gaugesolid.asp).

PROBLEMS

Inductor Design

9-1 Derive the expression for the rms current for the current waveform in Fig. 9-3.

9-2 In the design example of the inductor in this chapter, the core has an area $A_{core} = 93.1\,mm^2$, the magnetic path $\ell = 37.6\,mm$, and the relative permeability of the core material is $\mu_r = \mu_m / \mu_o = 5000$. Calculate the inductance with 31 turns if the air gap is not introduced in this core in the flux path.

9-3 In the inductor design presented in this chapter, what is the reluctance offered by the magnetic core as compared to that offered by the air gap?

9-4 In Problem 9-2, what is the maximum current that will cause the peak flux density to reach $0.25\,T$?

9-5 In the inductor designed in this chapter, what will be the inductance and the maximum current that can be passed without exceeding the $B_{\max}$ specified, if the air gap introduced by mistake is only one-half of the required value $\ell_g = 1\,mm$. What is the stored energy with $\ell_g = 0.5\,mm$ compared to that at $\ell_g = 1\,mm$?

Transformer Design

9-6 In the design example of the transformer in this chapter, the core has an area $A_{core} = 63.9\,mm^2$, the magnetic path $\ell = 31.2\,mm$, and the relative permeability of the core material is $\mu_r = \mu_m / \mu_o = 5000$. Calculate the peak magnetizing current at duty-ratio of 0.5.

9-7 What is the tertiary winding conductor diameter needed for the magnetizing current calculated in Problem 9-6?

9-8 Derive k_{conv} for a transformer in a Full-Bridge converter.

Chapter 10

SOFT-SWITCHING IN DC-DC CONVERTERS AND CONVERTERS FOR INDUCTION HEATING AND COMPACT FLUORESCENT LAMPS

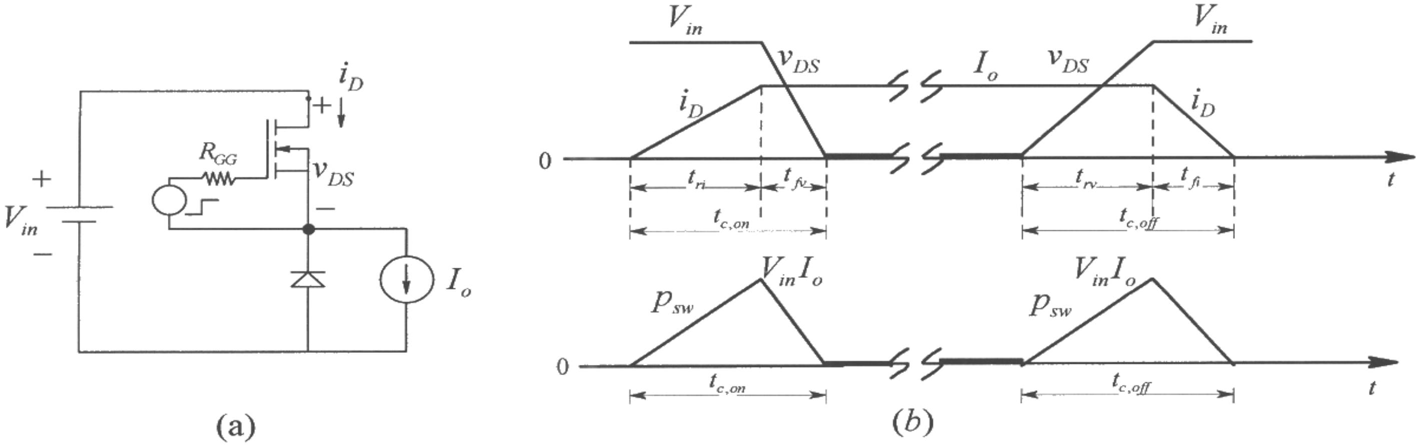
10-1 INTRODUCTION

In converters so far, we have discussed hard switching in the switching power-pole, as described in Chapter 2. In this chapter, we will look at the problems associated with hard switching, and some of the practical circuits where this problem can be minimized with soft-switching.

10-2 HARD-SWITCHING IN SWITCHING POWER-POLES

In the switching power-pole repeated in Fig. 10-1a, the hard-switching waveforms are as shown in Fig. 10-1b, which were discussed in Chapter 2. Because of the simultaneously high voltage and current associated with the transistor during the switching transition, the switching power losses in the transistor increase linearly proportional to the switching frequency and the times $t_{c(on)}$ and $t_{c(off)}$ shown in Fig. 10-1b, assuming an ideal diode

$$P_{sw} \propto f_s\left(t_{c(on)} + t_{c(off)}\right) \qquad (10\text{-}1)$$



(a) (b)

Figure 10-1 Hard switching in a power-pole.

In hard-switching converters, in addition to the switching power losses decreasing the energy efficiency, the other problems are device stresses, thermal management of power losses, and electromagnetic interference resulting from high di/dt and dv/dt due to fast transitions in the converter voltages and currents. The above problems are exacerbated by the presence of the stray capacitances and leakage inductances associated with the converter layout and the components.

In order to reduce the overall converter size, while maintaining high energy efficiency, the trend is to design dc-dc converters operating at as high a switching frequency as possible (typically 100-200 kHz in small power ratings), using fast-switching MOSFETs. At high switching frequency, the switching power losses become unacceptable if hard-switching is used, and hence soft-switching is often employed, as briefly described in this chapter.

The problems described above, associated with hard-switching, can be minimized by means of the following:

- Circuit layout to reduce stray capacitances and inductances
- Snubbers to reduce di/dt and dv/dt
- Gate-drive control to reduce di/dt and dv/dt
- Soft-switching

It is always recommended to have a layout to reduce stray capacitances and inductances. Snubbers, as describe in the Appendix on the accompanying CD, consist of passive elements (R, C and possibly a diode) to reduce di/dt and dv/dt during the switching transient, by shaping the switching trajectory. The trend in modern power electronics is to use snubbers only in transformer-isolated dc-dc converters, where the leakage inductance associated with the high-frequency transformer can be substantial, in spite of a good circuit layout. Generally, snubbers do not reduce the overall losses; rather they shift some of the switching losses in the transistor to the snubber resistor.

By controlling the gate voltage of MOSFETs and IGBTs, it is possible to slow down the turn-on and turn-off speed, thereby resulting in reduced di/dt and dv/dt, at the expense of higher switching losses in the transistor. The above techniques, at best, result in a partial solution to the problems of hard-switching.

However, there are certain topologies and control, as described in the next section, that allow soft-switching that essentially eliminate the drawbacks of hard-switching without creating new problems.

10-3 SOFT-SWITCHING IN SWITCHING POWER-POLES

There are many such circuits and control techniques proposed in the literature, most of which may make the problem of EMI and the overall losses worse due to large conduction losses in the switches and other passive components. Avoiding these topologies, only a few soft-switching circuits are practical.

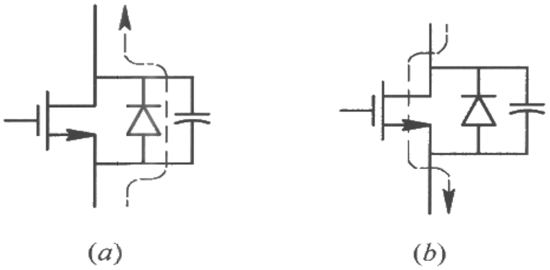
The goal in soft-switching is that the switching transition in the power-pole occurs under very favorable conditions, that is, the switching transistor has a zero voltage and/or zero current associated with it. Based on these conditions, the soft-switching circuits can be classified as follows:

- ZVS (zero voltage switching), and
- ZCS (zero current switching)

We will consider only the converter circuits using MOSFETs, which result in ZVS (zero voltage switching). The reason is that, based on Eq. 10-1, soft-switching is of interest at high switching frequencies where MOSFETs are used. In MOSFETs operating at high switching frequencies, a significant reduction of switching loss is achieved by not dissipating the charge associated with the junction capacitance inside the MOSFET each time it turns on. This implies that for a meaningful soft-switching, the MOSFETs should be turned on under a zero voltage switching (ZVS) condition. As we will see shortly, the turn-off also occurs at ZVS.

10-3-1 Zero Voltage Switching (ZVS)

To illustrate the ZVS principle, the intrinsic anti-parallel diode of the MOSFET is shown as being distinct in Figs. 10-2a and b, where a capacitor is used in parallel. This MOSFET is connected in a circuit such that before applying the gate voltage to turn the MOSFET on, the switch voltage is brought to zero and the anti-parallel diode is conducting as shown in Fig. 10-2a. This results in an ideal loss-less turn on at ZVS. At turn-off, as shown in Fig. 10-2b, the capacitor across the switch results in an essentially ZVS turn-off where the current through the MOSFET channel is removed while the voltage across the device remains small (essentially zero) due to the parallel capacitor. This ZVS principle is illustrated by modifying the synchronous-rectified Buck dc-dc converter, as discussed below.



(*a*) (*b*)

Figure 10-2 ZVS in a MOSFET.

10-3-2 Synchronous Buck Converter with ZVS

As discussed in section 3-10 of Chapter 3, a synchronous-rectified Buck dc-dc converter, used in applications where the output voltage is very low, is shown in Fig. 10-3a where the diode is replaced by another MOSFET and the two MOSFETs are provided complimentary gate signals q^+ and q^-. The waveforms associated with this synchronous Buck converter are shown in Fig. 10-3b, where the inductor is large such that the inductor-current ripple is small (shown by the solid curve in Fig. 10-3b), and the inductor current remains positive in the direction shown in Fig. 10-3a in the continuous conduction mode.

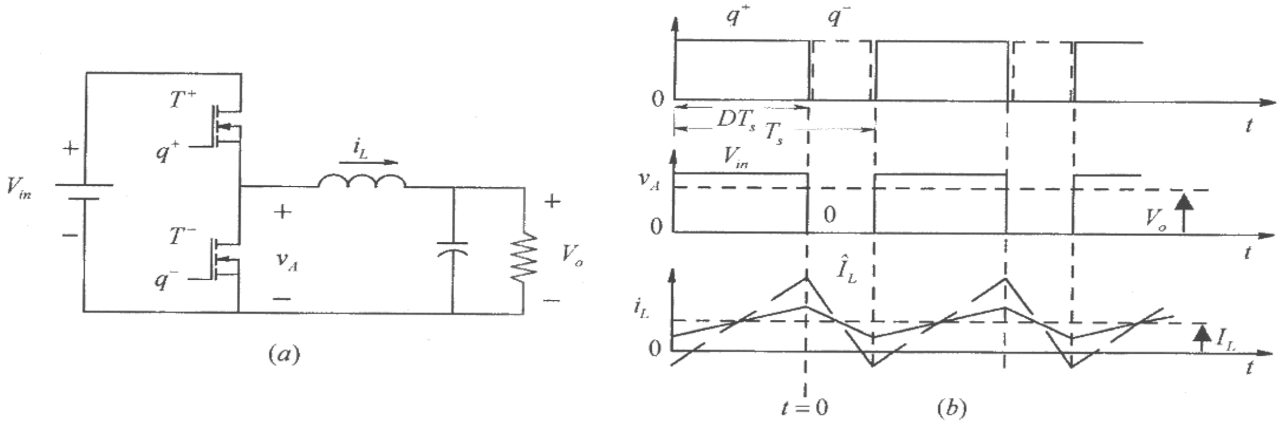


Figure 10-3 Synchronous-rectified Buck converter.

To achieve ZVS, the circuit of Fig. 10-3a is modified as shown in Fig. 10-4a by showing the internal diode of the MOSFET explicitly, and adding small external capacitances (in addition to the junction capacitances inherent in MOSFETs). The inductance value in this circuit is chosen to be much smaller such that the inductor current has a waveform shown dotted in Fig. 10-3b with a large ripple, such that the current i_L is both positive as well negative during every switching cycle.

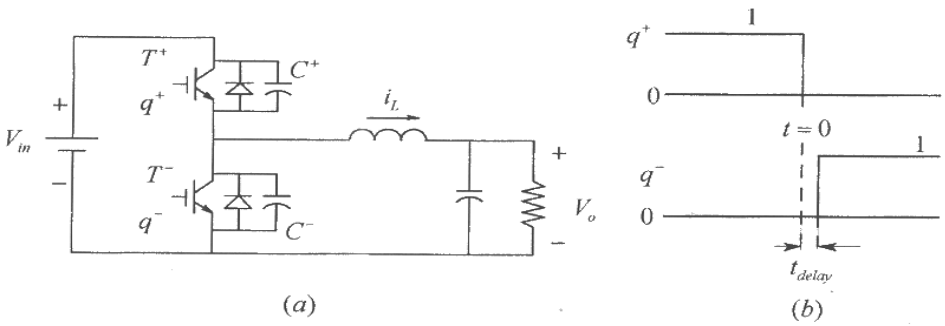


Figure 10-4 Synchronous-rectified Buck converter with ZVS.

We will consider the transition at the time $t=0$ labeled in Fig. 10-3b and Fig. 10-4b, when the inductor current is at its peak $\hat{I}_L$ in Fig. 10-4a. The gate signal q^+ of the transistor T^+, which is initially conducting $\hat{I}_L$, goes to zero, while q^- remains zero, as shown in Fig. 10-4b. During the transition time during which the current transfers from T^+ to T^- is very short, and it is reasonable to assume for discussion purposes that the inductor current remains constant at $\hat{I}_L$ as shown in Fig. 10-5a.

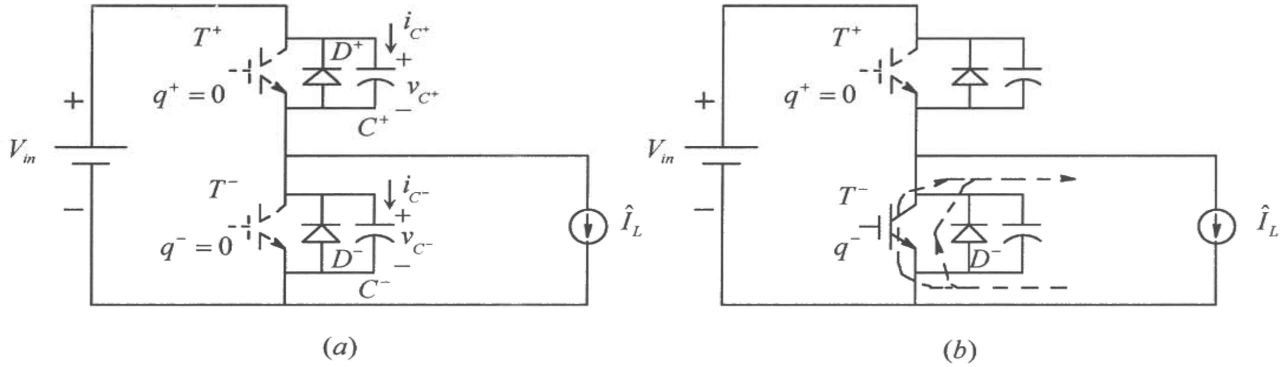


Fig. 10-5 Transition in synchronous-rectified Buck converter with ZVS.

In the circuit of Fig. 10-5a with both q and q^- equal to zero, initially $v_{C^+}(0)=0$ and $v_{C^-}(0)=V_{in}$, where from Kirchhoff's law these two voltages must add to the input voltage

$$v_{C^+}+v_{C^-}=V_{in} \tag{10-2}$$

As the current through T^+ declines, equal and opposite currents flow through the two capacitors in Fig. 10-5a, which can be derived from Eq. 10-2 as follows, assuming equal capacitances C: differentiating both sides of Eq. 10-2 and multiplying both sides by C

$$C\frac{d}{dt}v_{C^+}+C\frac{d}{dt}v_{C^-}=0 \tag{10-3}$$

$$i_{C^+}+i_{C^-}=0 \qquad \Rightarrow \qquad i_{C^+}=-i_{C^-} \tag{10-4}$$

As the current through T^+ declines, a positive i_{C^+} causes v_{C^+} to rise from 0, and a negative i_{C^-} causes v_{C^-} to decline from its initial value of V_{in}. If this voltage transition happens slowly compared to the current fall time of the MOSFET T^+, then the turn-off of T^+ is achieved at essentially zero voltage (ZVS). After the current through T^+ has gone to zero, applying the Kirchhoff's current law in Fig. 10-5a and using Eq. 10-4 results in

$$i_{C^+}=-i_{C^-}=\frac{\hat{I}_L}{2} \tag{10-5}$$

In Fig. 10-5a, during the turn-off transition of T^+, v_{C^+} rises to V_{in} and v_{C^-} declines to 0. The voltage v_{C^-} cannot become negative because of the diode D^- (assuming an ideal diode with zero forward voltage drop), which begins to conduct the entire i_L in Fig. 10-5b, marking the ZVS turn-off of T^+.

Once D^- begins to conduct, the voltage is zero across T^-, which is applied a gate signal q^- to turn-on, as shown in Fig. 10-4b, thus resulting in the ZVS turn-on of T^-. Subsequently, the entire inductor current begins to flow through the channel of T^- in Fig. 10-5b. The important item to note here is that the gate signal to T^- is appropriately delayed by an interval T_{delay} shown in Fig. 10-4b, making sure that q^- is applied after D^- begins to conduct.

The next half-cycle in this converter is similar with the ZVS turn-off of T^-, followed by the ZVS turn-on of T^+, facilitated by the negative peak of the inductor current.

Although this Buck converter results in ZVS turn-on and turn-off of both transistors, the inductor current has a large ripple, which will also make the size of the filter capacitor large since it has to carry the inductor current ripple. In order to make this circuit practical, the overall ripple that the output capacitor has to carry can be made much smaller (similar ripple reduction occurs in the current drawn from the input source) by interleaving of two or more such converters, as discussed in section 3-11 of Chapter 3.

10-3-3 Phase-Shift Modulated (PSM) DC-DC Converter

Another practical soft-switching technology is the phase-shift modulated (PSM) dc-dc converter shown in Fig. 10-6a.

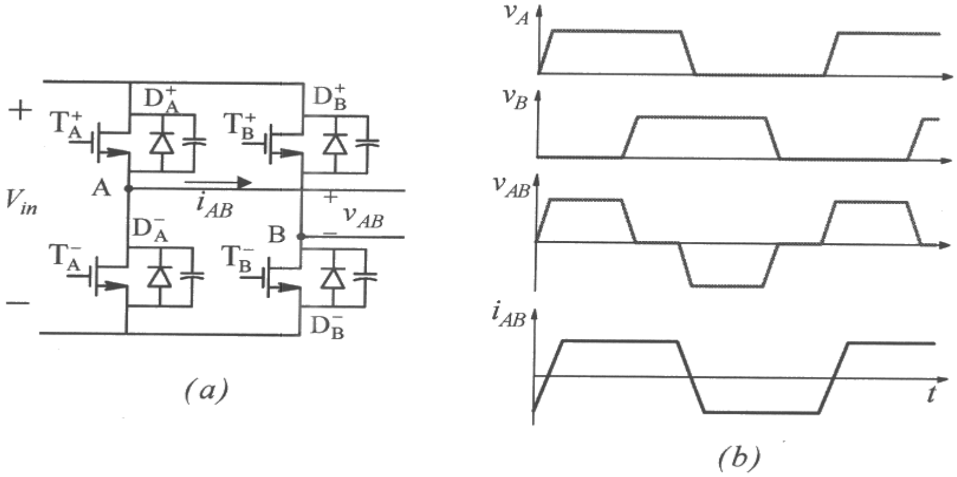


Figure 10-6 Phase-Shift Modulated (PSM) DC-DC Converter.

It is a variation of the PWM dc-dc converters discussed in Chapter 8. The switches in each power-pole of the PSM converter operate at nearly 50 percent duty-ratio and the regulation of the output voltage is provided by shifting the output of one switching power-pole with respect to the other, as shown in Fig. 10-6b, to control the zero-voltage intervals in the transformer primary voltage v_{AB}. To provide the ZVS turn-on and turn-off of switches, a capacitor is placed across each switch. This topology makes use of the transformer leakage inductance and the magnetizing current. The operation of this circuit and a superior hybrid topology shown in Fig. 10-7, patented by the University of Minnesota [3-5], are fully described in the Appendix to this chapter on the accompanying CD.

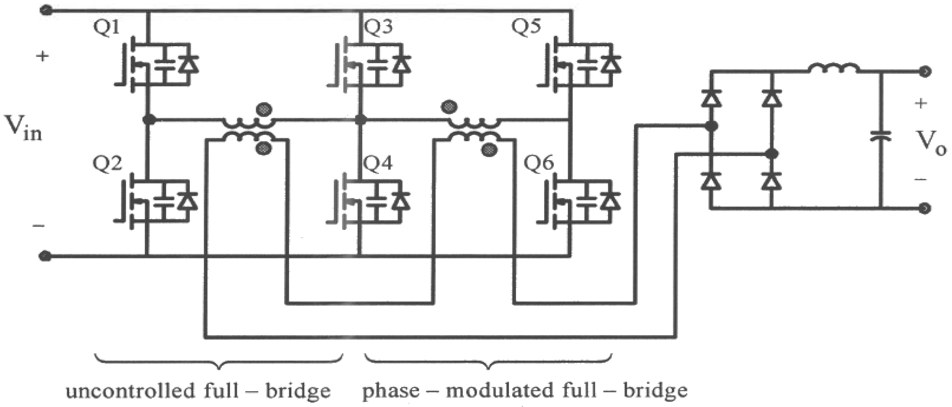


Figure 10-7 A superior hybrid topology to achieve ZVS down to no load [3-5].

10-4 INVERTERS FOR INDUCTION HEATING AND COMPACT FLUORESCENT LAMPS

It is possible to achieve soft-switching in converters for induction heating and compact fluorescent lamps. These converters are discussed in the Appendix to this chapter on the accompanying CD.

REFERENCES

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.
2. R. Ayyanar, N. Mohan, and E. Persson, " Soft-Switching in DC-DC Converters: Principles, Practical Topologies, Design Techniques, Latest Developments," Tutorial at IEEE-APEC 2002.
3. R. Ayyanar and N. Mohan, US Patent 6,310,785, University of Minnesota, 2001.
4. R. Ayyanar and N. Mohan, "Novel soft-switching dc-dc converter with full ZVS-range and reduced filter requirement – Part I: Regulated output applications", IEEE Transactions on Power Electronics, vol. 16 (2001), March 2001, p. 184-192.
5. R. Ayyanar and N. Mohan, "Novel soft-switching dc-dc converter with full ZVS-range and reduced filter requirement – Part II: Constant-input, variable output applications", IEEE Transactions on Power Electronics, vol. 16 (2001), March 2001, p. 193-200.

PROBLEMS

10-1 In a synchronous-rectified Buck converter with ZVS shown in Fig. 10-4a, $V_{in} = 12V$, $V_o = 5V$, $f_s = 100 kHz$, and the maximum load is $20W$. Calculate the filter inductance such that the negative peak current is at least 1.5Amps.

10-2 In Problem 10-1, calculate the capacitances across the MOSFETs if the charge/discharge time is to be no more than $0.5\,\mu s$.

Chapter 11

ELECTRIC MOTOR DRIVES

11-1 INTRODUCTION

Motor drives (ac and dc) form an extremely important application area of power electronics with market value of tens of billions dollars annually in applications described in Chapter 1. Figure 11-1 shows the block diagram of an electric-motor drive, or for short, an electric drive. In response to an input command, electric drives efficiently control the speed and/or the position of the mechanical load. The controller, by comparing the input command for speed and/or position with the actual values measured through sensors, provides appropriate control signals to the power-processing unit (PPU) consisting of power semiconductor devices.

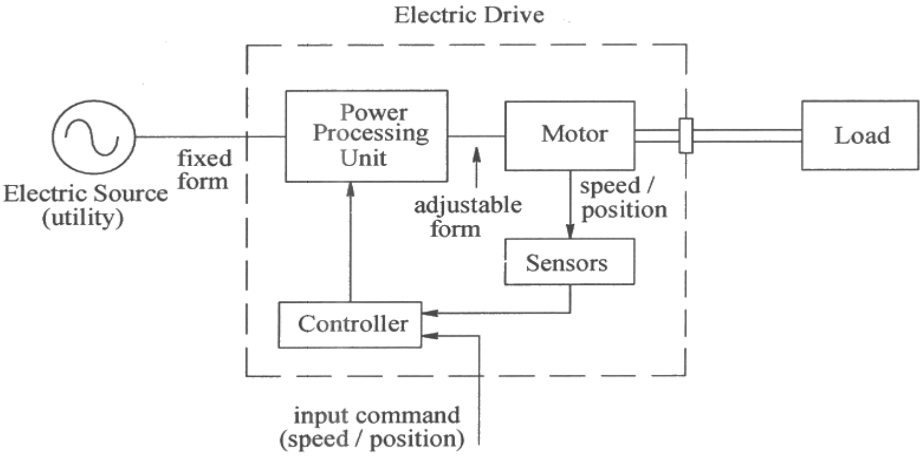


Figure 11-1 Block diagram of an electric drive system.

As Fig. 11-1 shows, the power-processing unit gets its power from the utility source with single-phase or three-phase sinusoidal voltages of a fixed frequency and constant amplitude. The power-processing unit, in response to the control inputs, efficiently converts these fixed-form input voltages into an output of the appropriate form (in frequency, amplitude, and the number of phases) that is optimally suited for operating the motor. The input command to the electric drive in Fig. 11-1 may come from a process computer, which considers the objectives of the overall process and issues a command to control the mechanical load. However, in general-purpose applications, electric drives operate in an open-loop manner without any feedback.

Prior to discussing the need for power electronics in electric drives for speed and position control of mechanical systems, we will briefly examine the requirements of mechanical systems, and various types of electric machines in terms of their terminal characteristics in steady state in order to determine the voltage and current ratings in designing the power electronics interface.

11-2 MECHANICAL SYSTEM REQUIREMENTS

Electric drives must satisfy the requirements of torque and speed imposed by mechanical loads connected to them. Most electric motors are of rotating type.

11-2-1 Rotational Motor-Load Systems

To understand rotating systems, consider a lever, pivoted and free to move. When an external force f is applied in a *perpendicular* direction at a radius r from the pivot, then the torque acting on the lever is

$$\underset{[Nm]}{T} = \underset{[N]}{f}\ \underset{[m]}{r} \qquad (11\text{-}1)$$

which acts in a counter-clockwise direction, considered here to be positive.

In a rotational system, the angular acceleration due to a net torque acting on it is determined by its moment-of-inertia J. The net torque T_J acting on the rotating body of inertia J causes it to accelerate. Similar to systems with linear motion, Newton's Law in rotational systems becomes

$$T_J = J\alpha \qquad (11\text{-}2)$$

where the angular acceleration $\alpha(= d\omega_m / dt)$ in rad/s^2 is

$$\alpha = \frac{d\omega_m}{dt} = \frac{T_J}{J} \qquad (11\text{-}3)$$

In MKS units, a torque of $1\,Nm$, acting on an inertia of $1\,kg \cdot m^2$ results in an angular acceleration of $1\,rad/s^2$.

In systems such as the one shown in Fig. 11-2a, the motor produces an electromagnetic torque T_{em}. The bearing friction and wind resistance (drag) can be combined with the load torque T_L opposing the rotation. In most systems, we can assume that the rotating part of the motor with inertia J_M is rigidly coupled (without flexing) to the load inertia J_L. The net torque, the difference between the electromagnetic torque developed by the motor and the load torque opposing it, causes the combined inertias of the motor and the load to accelerate in accordance with Eq. 11-3:

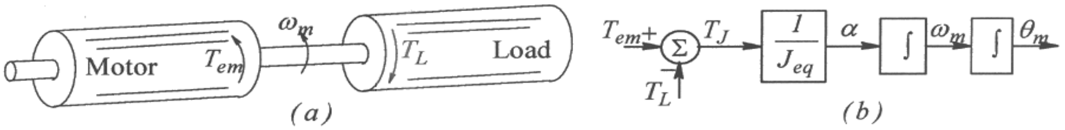


Figure 11-2 Motor and load torque interaction with a rigid coupling.

$$\frac{d}{dt}\omega_m = \frac{T_J}{J_{eq}} \tag{11-4}$$

where the net torque $T_J = T_{em} - T_L$ and the equivalent combined inertia $J_{eq} = J_M + J_L$.

Eq. 11-4 shows that the net torque is the quantity that causes acceleration, which in turn leads to changes in speed and position. Integrating the acceleration $\alpha(t)$ with respect to time,

$$\text{Speed } \omega_m(t) = \omega_m(0) + \int_0^t \alpha(\tau)d\tau \tag{11-5}$$

where $\omega_m(0)$ is the speed at t=0 and τ is a variable of integration. Further integrating $\omega_m(t)$ in Eq. 11-5 with respect to time yields

$$\theta_m(t) = \theta_m(0) + \int_0^t \omega_m(\tau)d\tau \tag{11-6}$$

where $\theta_m(0)$ is the position at $t = 0$, and τ is again a variable of integration. Eqs. 11-4 through 11-6 indicate that torque is the fundamental variable for controlling speed and position. Eqs. 11-4 through 11-6 can be represented in a block-diagram form, as shown in Fig. 11-2b.

11-2-2 Power and Energy in Rotational Systems

In the rotational system shown in Fig. 11-3, if a net torque T causes the cylinder to rotate by a differential angle $d\theta_m$, the differential work done is

$$dW = T\,d\theta_m \tag{11-7}$$

If this differential rotation takes place in a differential time *dt,* the power can be expressed as

$$p = \frac{dW}{dt} = T\frac{d\theta_m}{dt} = T\,\omega_m \tag{11-8}$$

where $\omega_m = d\theta_m / dt$ is the angular speed of rotation.

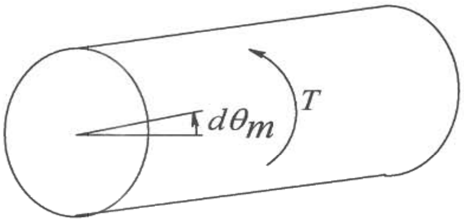


Figure 11-3 Torque, work and power.

11-2-3 Electrical Analogy

An analogy with electrical circuits can be very useful when analyzing mechanical systems. A commonly used analogy, though not a unique one, is to relate mechanical and electrical quantities as shown in Table 11-1.

Table 11-1 Torque–Current Analogy

Mechanical System	Electrical System
Torque (T)	Current (i)
Angular speed (ω_m)	Voltage (v)
Angular displacement (θ_m)	Flux linkage (ψ)
Moment of inertia (J)	Capacitance (C)

For the mechanical system shown in Fig. 11-2a, Fig. 11-4 shows the electrical analogy, where torques are represented by current sources. Inertias are represented by capacitors, from its node to a reference (ground) node, and the two capacitors representing the two inertias are combined to result in a single equivalent capacitor.

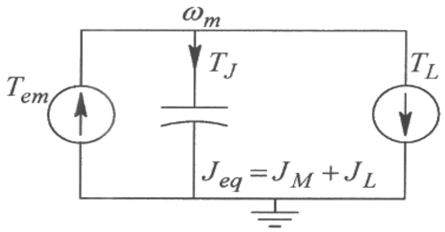


Figure 11-4 Electrical Analogy.

11-3 INTRODUCTION TO ELECTRIC MACHINES AND THE BASIC PRINCIPLES OF OPERATION

Electric machines, as motors, convert electrical power input into mechanical output, as shown in Fig. 11-5. Machines may be operated solely as generators, but they also enter the generating mode when slowing down (during regenerative braking) where the power flow is reversed. In this section, we will briefly look at the basic structure and the fundamental principles of the electromagnetic interactions that govern their operation.

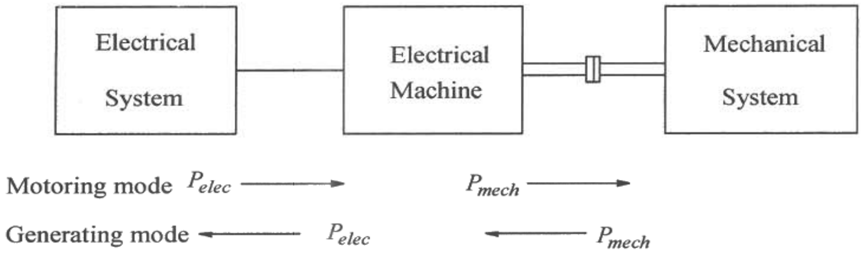

Electrical System
Electrical Machine
Mechanical System
Motoring mode P_{elec}
P_{mech}
Generating mode
P_{elec}
P_{mech}

Figure 11-5 Electric machine as an energy converter.

There are two basic principles that govern electric machines' operation to convert between electric energy and mechanical work:

1) A force is produced on a current-carrying conductor when it is subjected to an *externally-established* magnetic field.
2) An emf is induced in a conductor moving in a magnetic field.

11-3-1 Electromagnetic Force

Consider a conductor of length ℓ in Fig. 11-6a. The conductor is carrying a current i and is subjected to an *externally-established* magnetic field of a uniform flux-density B perpendicular to the conductor length. A force f_{em} is exerted on the conductor due to the electromagnetic interaction between the external magnetic field and the conductor current. The magnitude of this force f_{em} is given as

$$\underbrace{f_{em}}_{[N]} = \underbrace{B}_{[T]}\,\underbrace{i}_{[A]}\,\underbrace{\ell}_{[m]} \tag{11-9}$$

As shown in Fig. 11-6a, the direction of the force is perpendicular to the directions of both i and B. To obtain the direction of this force, we will superimpose the flux lines produced by the conductor current, which are shown in Fig. 11-6a. The flux lines add up on the right side of the conductor and subtract on the left side, as shown in Fig. 11-6b. Therefore, the force f_{em} acts *from the higher concentration of flux lines to the lower concentration*, that is, from right to left in this case.

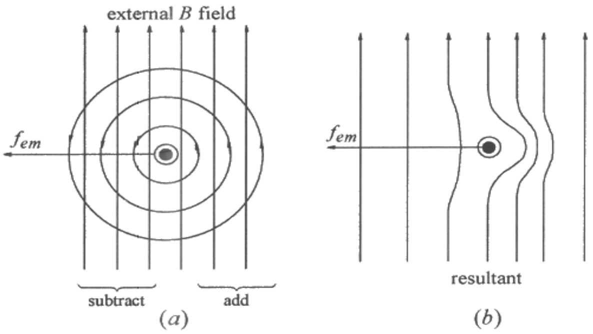

external B field
f_{em}
subtract
add
(a)
f_{em}
resultant
(b)

Figure 11-6 Electric force on a current-carrying conductor in a magnetic field.

11-3-2 Induced EMF

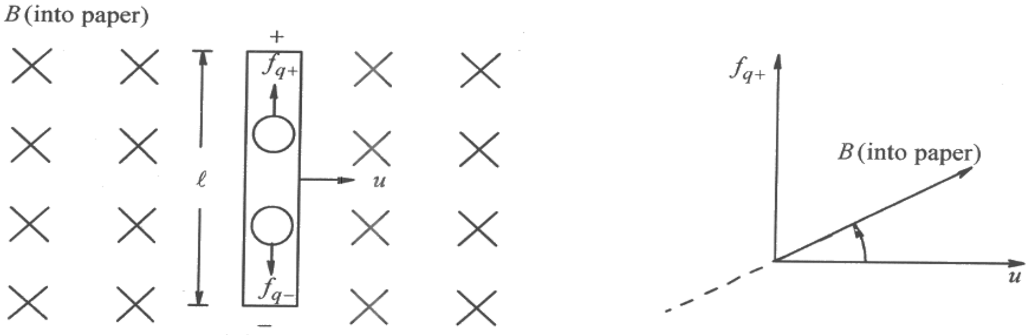
In Fig. 11-7a, a conductor of length ℓ is moving to the right at a speed u. The B-field is uniform and is perpendicularly directed into the paper plane. The magnitude of the induced emf at any instant of time is then given by

$$\underbrace{e}_{[V]} = \underbrace{B}_{[T]}\,\underbrace{l}_{[m]}\,\underbrace{u}_{[m/s]} \tag{11-10}$$

The polarity of the induced emf can be established as follows: due to the conductor motion, the force on a charge q (positive, or negative in the case of an electron) within the conductor can be written as

$$f_q = q(\mathbf{u} \times \mathbf{B}) \tag{11-11}$$

where the speed and the flux density are shown by bold letters to imply that these are vectors and their cross product determines the force. Since **u** and **B** are orthogonal to each other, as shown in Fig. 11-7b, the force on a positive charge is upward. Similarly, the force on an electron will be downwards. Thus, the upper end will have a positive potential with respect to the lower end. This induced emf across the conductor is independent of the current that would flow if a closed path were to be available (as would normally be the case). With the current flowing, the voltage across the conductor will be the induced-emf $e(t)$ in Eq. 11-10 minus the voltage drops across the conductor resistance and inductance.



(a) (b)

Figure 11-7 Conductor moving in a magnetic field.

11-3-3 Basic Structure

Based on the above basic principles, all machines have a stationary part, called the stator, and a rotating part, called the rotor, separated by an air gap, thereby allowing the rotor to rotate freely on a shaft, supported by bearings. This is shown by the cross-section of the machine in Fig. 11-8a, where the stator is firmly affixed to a foundation to prevent it from turning.

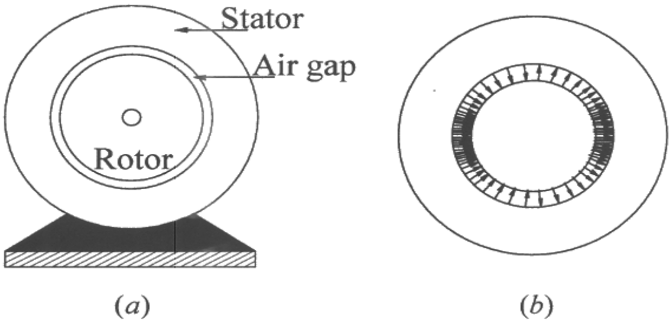


Figure 11-8 Cross-section of the machine seen from one side.

In electric machines, a magnetic field is produced either by permanent magnets or by windings that are supplied currents to produce radial flux-lines through the air gap, as shown in Fig. 11-8b. In order to require small ampere-turns to create flux lines crossing the air gap, both the rotor and the stator are made up of high permeability ferromagnetic materials and the length of the air gap is kept as small as possible. In machines with ratings under 10 *kW* in ratings, a typical length of the air gap is about 1 *mm*, which is shown highly exaggerated for ease of drawing.

In the next sections, we will briefly examine commonly used machines: dc, permanent-magnet ac, and induction.

11-4 DC MOTORS

DC motors were widely used in the past for all types of applications, and they continue to be used in applications to control speed and position. There are two designs of dc machines: stators consisting of either permanent magnets or a field winding. The power-processing units can also be classified into two categories: switch-mode power converters that operate at a high switching frequency as discussed in the next Chapter 12, or line-commutated, thyristor converters, which are discussed later in Chapter 14. In this chapter, our focus will be on small servo-drives, which usually consist of permanent-magnet motors supplied by switch-mode power electronic converters.

11-4-1 Structure of DC Machines

Fig. 11-9 shows a cut-away view of a dc motor. It shows a permanent-magnet stator, a rotor that carries a winding, a commutator, and the brushes. In dc machines, the stator establishes a uniform flux ϕ_f in the air gap in the radial direction (the subscript "f" is for field). If permanent magnets like those shown in Fig. 11-9 are used, the air gap flux density established by the stator remains constant. A field winding whose current can be varied can be used to achieve an additional degree of control over the air gap flux density.

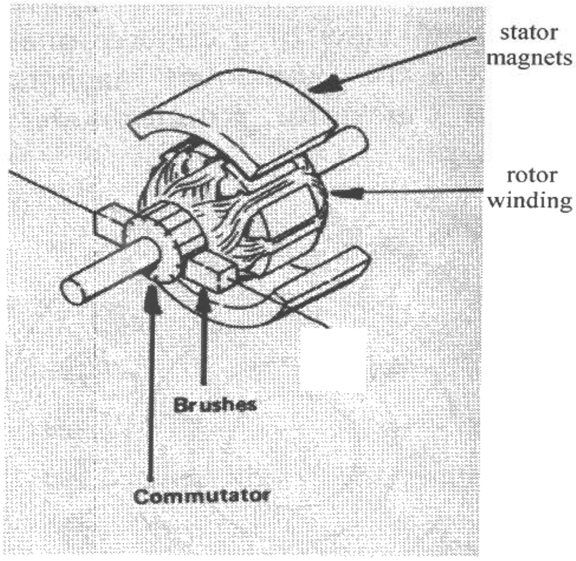


Figure 11-9 Exploded view of a dc motor; source: Engineering Handbook by Electro-Craft Corp.

As shown in Fig. 11-9, the rotor slots contain a winding, called the armature winding, which handles electrical power for conversion to (or from) mechanical power at the rotor shaft. In addition, there is a commutator affixed to the rotor. On its outer surface, the commutator contains copper segments, which are electrically insulated from each other by means of mica or plastic. The coils of the armature winding are connected to these commutator segments so that a stationary dc source can supply voltage and current to the rotating cummutator by means of stationary carbon brushes which rest on top of the commutator. The wear due to the mechanical contact between the commutator and the brushes requires periodic maintenance, which is the main drawback of dc machines.

11-4-2 Operating Principles of DC Machines

As Fig. 11-10 pictorially shows, the commutator and the brushes in dc machines act as a "mechanical rectifier" and convert a dc current i_a supplied by a stationary dc source into a current that changes direction in the armature coil every half revolution of the rotor.

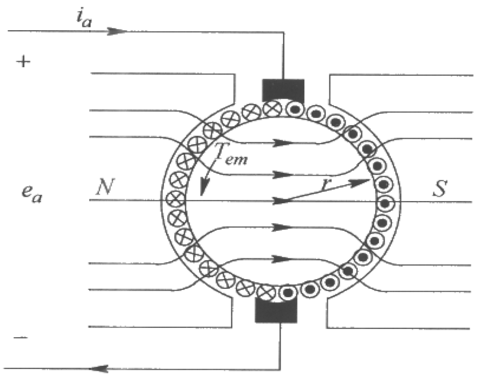


Figure 11-10 DC machine schematic representation.

All conductors under a stator pole have currents in the same direction but the current direction reverses when the conductors reach the other pole. This is needed so that the forces produced on each conductor are in the same direction and add up to yield the total torque. Similarly, all conductors under a pole have induced emfs of the same polarity, which changes in polarity every half revolution of the rotor when the conductors reach the other pole.

The above description shows that the magnitude and the direction of the electromagnetic torque depend on the armature current i_a. Therefore, in a permanent-magnet dc machine, the electromagnetic torque produced by the machine is linearly related to a machine torque-constant k_T, which is unique to a given machine and is specified in its data sheets

$$T_{em} = k_T\, i_a \qquad (11\text{-}12)$$

Similarly, the induced emf e_a depends only on the rotational speed ω_m, and can be related to it by a voltage-constant k_E, which is unique to a given machine and specified in its data sheets

$$e_a = k_E\, \omega_m \qquad (11\text{-}13)$$

Equating the mechanical power ($\omega_m T_{em}$) to the electrical power ($e_a i_a$), the torque-constant k_T and the voltage-constant k_E are exactly the same numerically in MKS units

$$k_T = k_E \qquad (11\text{-}14)$$

Reversing the Torque Direction. The direction of the armature current i_a determines the direction of currents through the conductors. Therefore, the direction of the electromagnetic torque produced by the machine also depends on the direction of i_a. This explains, how a dc machine while rotating in a forward or reverse direction can be made to go from motoring mode (where the speed and torque are in the same direction) to its generator mode (where the speed and torque are in the opposite direction) by reversing the direction of i_a.

Reversing the Direction of Rotation. Applying a reverse-polarity dc voltage to the armature terminals makes the armature current flow in the opposite direction. Therefore, the electromagnetic torque is reversed, reversing the direction of rotation and the polarity of induced emfs in conductors, which depends on the direction of rotation.

Four-Quadrant Operation. The above discussion shows that a dc machine can easily be made to operate as a motor or as a generator in forward or reverse direction of rotation.

11-4-3 DC-Machine Equivalent Circuit

It is convenient to discuss a dc machine in terms of its equivalent circuit of Fig. 11-11, which shows conversion between electrical and mechanical power. The armature current i_a produces the electromagnetic torque $T_{em}(=k_T i_a)$, represented by a dependent current-source necessary to rotate the mechanical load at a speed ω_m. Across the armature terminals, the rotation at the speed of ω_m induces a voltage, called the back-emf $e_a(=k_E\omega_m)$, represented by a dependent voltage-source.

On the electrical side, the applied voltage v_a overcomes the back-emf e_a and causes the current i_a to flow. Recognizing that there is a voltage drop across both the armature winding resistance R_a (which includes the voltage drop across the carbon brushes) and the armature winding inductance L_a, we can write the equation of the electrical side as

$$v_a = e_a + R_a \mathrm{i}_a + L_a \frac{di_a}{dt} \tag{11-15}$$

On the mechanical side, the electromagnetic torque produced by the motor overcomes the mechanical-load torque T_L to produce acceleration:

$$\frac{d\omega_m}{dt} = \frac{1}{J_{eq}}(T_{em} - T_L) \tag{11-16}$$

where J_{eq} is the total effective value of the combined inertia of the dc machine and the mechanical load.

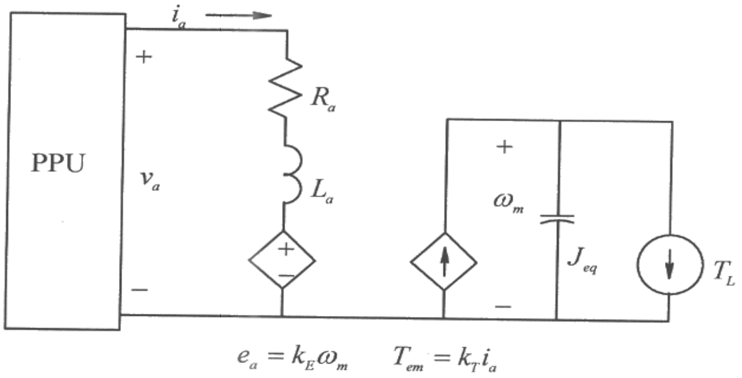


Figure 11-11 DC motor equivalent circuit.

11-4-4 Torque-Speed Characteristics

Note that the electric and the mechanical systems are coupled. The torque T_{em} in the mechanical system (Eq. 11-12) depends on the electrical current i_a. The back-emf e_a in the electrical system (Eq. 11-13) depends on the mechanical speed ω_m. The electrical power absorbed from the electrical source by the motor is converted into mechanical power and vice versa. In a dc steady state, with a voltage V_a applied to the armature terminals, and a load-torque T_L being supplied to the load, the equivalent circuit is as shown in Fig. 11-12a, where the inductance L_a (not shown) in the electrical portion and the capacitance (shown dotted) representing J_{eq} in the mechanical portion of the circuit do not play a role in dc steady state. Hence, in Fig. 11-12

$$I_a = \frac{T_{em}(=T_L)}{k_T} \tag{11-17}$$

$$\omega_m = \frac{E_a}{k_E} = \frac{V_a - R_a I_a}{k_E} = \frac{V_a - R_a\left(T_{em}/k_T\right)}{k_E} \tag{11-18}$$

Based on Eqs. 11-17 and 11-18, the steady state torque-speed characteristics for various values of V_a are plotted in Fig. 11-12b.

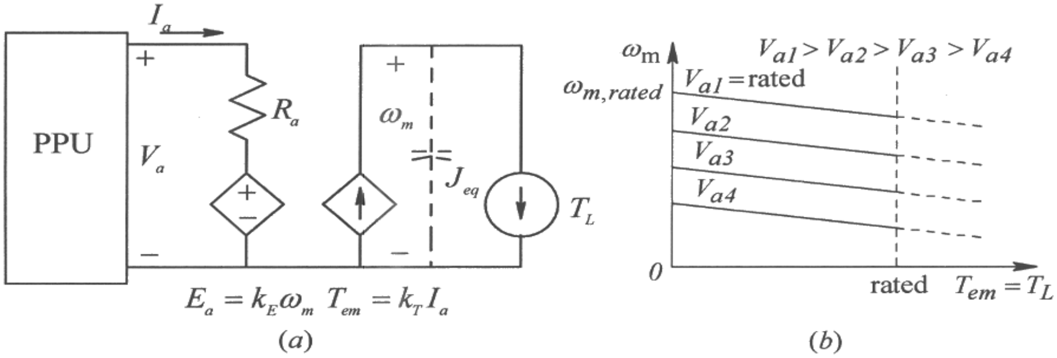


Figure 11-12 DC motor in the dc steady state.

11-5 PERMANENT-MAGNET AC MACHINES

We will now study an important class of ac drives, namely sinusoidal-waveform, permanent-magnet ac (PMAC) drives, which are used in applications where a high efficiency and a high power density are required in controlling the speed and position. In trade literature, they are also called "brushless dc" drives. We will examine these machines for speed and position control applications, usually in small (< 10 *kW*) power ratings, where these drives have three-phase ac stator windings and the rotor has dc excitation in the form of permanent magnets. In such drives, the stator windings of the machine are supplied by controlled currents, which require a closed-loop operation, as shown in the block diagram of Fig. 11-13. The discussion of PMAC drives also lends itself to the analysis of line-connected synchronous machines, which are used in very large ratings in the central power plants of utilities to generate electricity.

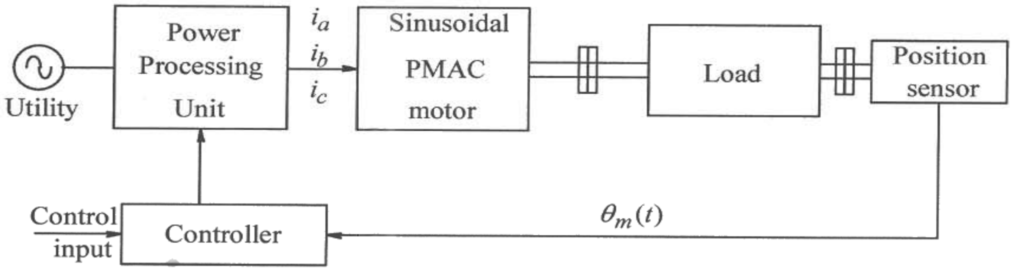

Utility
Power Processing Unit
i_a
i_b
i_c
Sinusoidal PMAC motor
Load
Position sensor
Control input
Controller
$\theta_m(t)$

Figure 11-13 Block diagram of the closed loop operation of a PMAC drive.

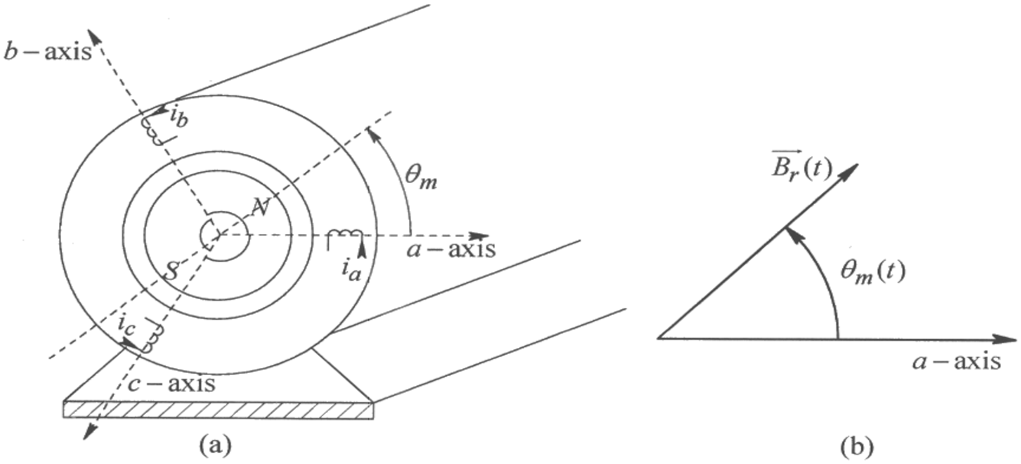
11-5-1 The Basic Structure of Permanent-Magnet AC Machines

We will consider 2-pole machines, like the one shown schematically in Fig. 11-14a. This analysis can be generalized to *p*-pole machines where $p > 2$. The stator contains three-phase, wye-connected windings shown in the cross-section of Fig. 11-14a, each of which produce a sinusoidally-distributed flux-density distribution in the air gap, when supplied by a current.

11-5-2 Principle of Operation

The permanent-magnet pole pieces mounted on the rotor surface are shaped to ideally produce a sinusoidally-distributed flux density in the air gap. The rotor flux-density distribution (represented by a vector $\vec{B}_r$) peaks at an axis that is at an angle $\theta_m(t)$ with respect to the *a*-axis of phase winding *a*, as shown in Fig. 11-14b. As the rotor turns, the entire rotor-produced flux density distribution in the air gap rotates with it and "cuts" the stator-winding conductors and produces emf in phase windings that are sinusoidal functions of time. In the ac steady state, these voltages can be represented by phasors.

Considering phase-a as the reference in Fig. 11-14b, the induced voltage in it due to the rotor flux cutting it can be expressed as


$b-$axis
i_b
θ_m
N
S
i_a
$a-$axis
i_c
$c-$axis
$\overrightarrow{B_r}(t)$
$\theta_m(t)$
$a-$axis

(a)

(b)

Figure 11-14 Two-pole PMAC machine.

$$\overline{E}_{ma} = E_{rms}\angle 0^0 \tag{11-19}$$

It should be noted that the induced voltage in phase-a peaks when the rotor-flux peak in Fig. 11-14 is pointing downward, 90^0 before it reaches the phase-a magnetic axis. Since the flux produced by the permanent magnets on the rotor is constant, the rms magnitude of the induced voltage in each stator phase is linearly related to the rotational speed ω_m by a per-phase voltage-constant $k_{E,\,phase}$

$$E_{rms} = k_{E,\,phase}\,\omega_m \tag{11-20}$$

An important characteristic of the machines under consideration is that they are supplied through a current-regulated power-processing unit shown in Fig. 11-13, which controls the currents i_a, i_b, and i_c supplied to the stator at any instant of time. To optimize such that the maximum torque-per-ampere is produced, each phase current in ac steady state is controlled in phase with the induced voltage. Therefore, with the voltage expressed in Eq. 11-19, the current in ac steady state is

$$\overline{I}_a = I_{rms}\angle 0^0 \tag{11-21}$$

In ac steady state, accounting all three-phases, the input electric power, supplied by the current in opposition to the induced back-emf, equals the mechanical output power. Using Eqs. 11-19 through 11-21

$$T_{em}\omega_m = 3\underbrace{\left(k_{E,\,phase}\,\omega_m\right)}_{E_{rms}} I_{rms} \tag{11-22}$$

The torque contribution of each phase can be written as

$$T_{em,1-phase} = \frac{T_{em}}{3} = k_{E,\,phase}\,I_{rms} \tag{11-23}$$

In Eq. 11-23, the constant that relates the rms current to the per-phase torque is the per-phase torque-constant $k_{T,\,phase}$. Therefore, similar to that in dc machines, in MKS units

$$k_{T,\,phase} = k_{E,\,phase} \tag{11-24}$$

At this point, we should note that PMAC drives constitute a class, which we will call *self-synchronous* motor drives, where the term "*self*" is added to distinguish these machines from the conventional synchronous machines. The reason for this is as follows: in PMAC drives, the stator phase currents are synchronized to the mechanical position of the rotor such that, for example, the current into phase-a, in order to be in phase with the induced-emf, peaks when the rotor-flux peak is pointing downward, 90^0 before it reaches the phase-a magnetic axis. This explains the necessity for the rotor-position sensor, unless the rotor position is mathematically computed by sensed voltages and currents.

11-5-3 Mechanical System of PMAC Drives

The electromagnetic torque acts on the mechanical system connected to the rotor, and the resulting speed ω_m can be obtained from the equation below:

$$\frac{d\omega_m}{dt} = \frac{T_{em} - T_L}{J_{eq}} \quad \Rightarrow \quad \omega_m(t) = \omega_m(0) + \frac{1}{J_{eq}} \int_o^t (T_{em} - T_L) \cdot d\tau \tag{11-25}$$

where J_{eq} is the combined motor-load inertia and T_L is the load torque, which may include friction. The rotor position $\theta_m(t)$ is

$$\theta_m(t) = \theta_m(0) + \int_o^t \omega_m(\tau) \cdot d\tau \tag{11-26}$$

where $\theta_m(0)$ is the rotor position at time $t=0$.

11-5-4 PMAC Machine Equivalent Circuit

Similar to a dc machine, it is convenient to discuss a PMAC machine in terms of its equivalent circuit of Fig. 11-15a, which shows conversion between electrical and mechanical power. In the ac steady state, using phasors, the current $\bar{I}_a$ is ensured to be in phase with the phase-a induced voltage $\bar{E}_{ma}$ by the feedback control. The phase currents produce the total electromagnetic torque $T_{em}(=3k_{T,phase}I_{rms})$, represented by a dependent current-source, necessary to rotate the mechanical load at a speed ω_m. The induced back-emf $\bar{E}_{ma} = E_{rms}\angle 0^0$, whose rms magnitude is linearly proportional to the speed of rotation ω_m, is represented by a dependent voltage-source.

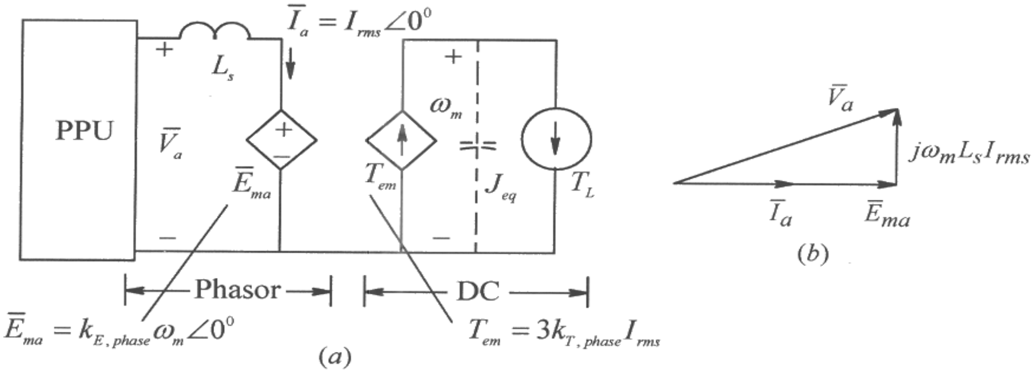


Figure 11-15 Equivalent circuit diagram and the phasor diagram of PMAC (2 pole).

On the electrical side, the applied voltage $\bar{V}_a$ in Fig. 11-15a overcomes the back-emf $\bar{E}_{ma}$ and causes the current $\bar{I}_a$ to flow. The frequency of the phasors in Hz equals $\omega_m/(2\pi)$

in a 2-pole PMAC machines. There is a voltage drop across both the per-phase stator winding resistance R_s (neglected here) and a per-phase inductance L_s, which is the sum of the leakage inductance caused by the leakage flux of the stator winding, and the effect of the combined flux produced by the currents flowing in the stator phases. On the mechanical side in Fig. 11-15a in steady state, the capacitance representing J_{eq} in the mechanical portion of the circuit is of no effect, and $T_{em} = T_L$.

Note that the electric and the mechanical systems are coupled. In the electrical system, the back-emf $\overline{E}_{ma}$ magnitude (Eq. 11-20) depends on the mechanical speed ω_m. In the mechanical system, the torque T_{em} (Eq. 11-23) depends on the magnitude of the electrical current $\overline{I}_a$, which depends on the load torque being demanded of the machine. The electrical power absorbed from the electrical source by the motor is converted into mechanical power and vice versa. The phasor diagram, neglecting R_s, is shown in Fig. 11-15b.

11-5-5 PMAC Torque-Speed Characteristics

In PMAC machines, the speed is independent of the electromagnetic torque developed by the machine, as shown in Fig. 11-16a, and depends on the frequency of voltages and currents applied to the stator phases of the machine.

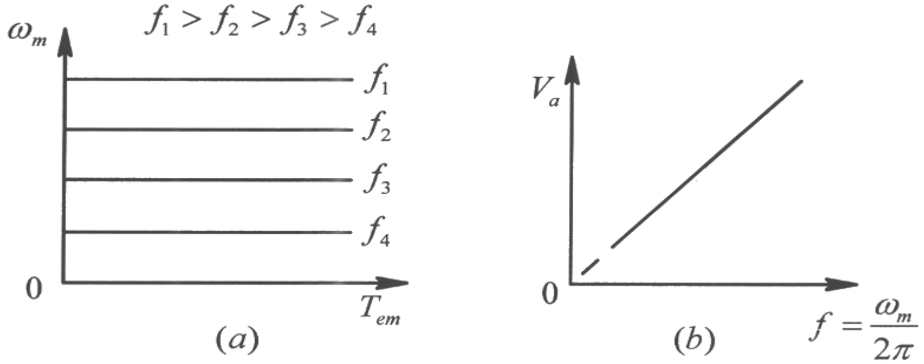


Figure 11-16 Torque-speed characteristics and the voltage versus frequency in PMAC.

In the per-phase equivalent circuit of Fig. 11-15a and the phasor diagram of Fig. 11-15b, the back-emf is proportional to the speed ω_m. Similarly, since the electrical frequency is linearly related to ω_m, the voltage drop across L_s is also proportional to ω_m. Therefore, neglecting the per-phase stator winding resistance R_s, in the phasor diagram of Fig. 11-15b, the voltage phasors are all proportional to ω_m, requiring that the per-phase voltage magnitude that the power-processing unit needs to supply is proportional to the speed ω_m, as plotted in Fig. 11-16b. This relationship between the voltage and speed shown in Fig. 11-16b is approximate. A substantially higher voltage, called the voltage boost, above that indicated by the dotted line, is needed at very low speeds, where the voltage drop across the stator winding resistance R_s becomes substantial at higher torque loading, and hence cannot be neglected.

11-5-6 The Controller and the Power-Processing Unit (PPU)

As shown in the block diagram of Fig. 11-13, the task of the controller is to dictate the switching in the power-processing unit, such that the desired currents are supplied to the PMAC motors. The reference torque signal is generated from the outer speed and position loops discussed in Chapter 13. The rotor position θ_m is measured by the position sensor connected to the shaft. Knowing the torque constant $k_{T,phase}$ allows us to calculate the rms value of the reference current from Eq. 11-23. Knowing the current rms value and θ_m allows the reference currents for the three phases to be calculated, which the PPU delivers at any instant of time.

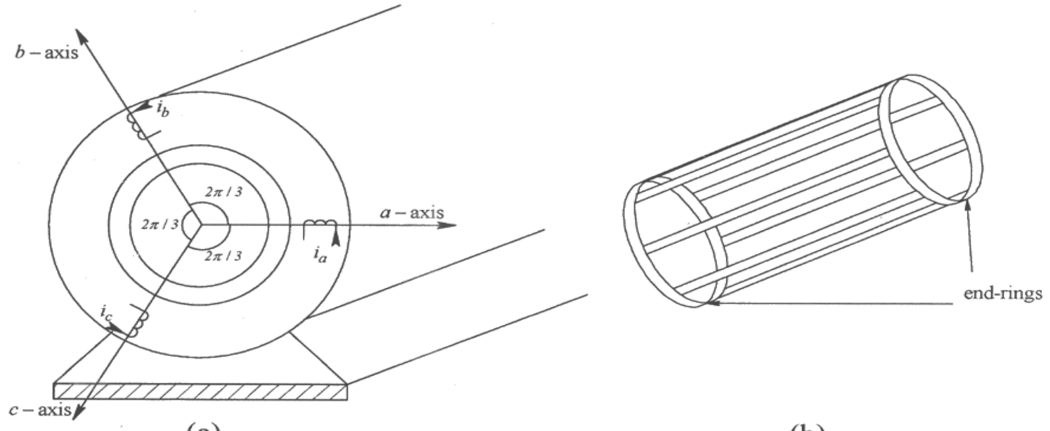
11-6 INDUCTION MACHINES

Induction motors with squirrel-cage rotors are the workhorses of industry because of their low cost and rugged construction. When operated directly from line voltages (a 50- or 60-*Hz* utility input at essentially a constant voltage), induction motors operate at a nearly constant speed. However, by means of power electronic converters, it is possible to vary their speed efficiently.

11-6-1 Structure of Induction Machines

The stator of an induction motor consists of three-phase windings, distributed in the stator slots. These three windings are displaced by 120° in space with respect to each other, as shown by their axes in Fig. 11-17a.

The rotor, consisting of a stack of insulated laminations, has electrically conducting bars of copper or aluminum inserted (molded) through it, close to the periphery in the axial



(a) (b)

Figure 11-17 (a) Three-phase stator; (b) squirrel-cage rotor.

direction. These bars are electrically shorted at each end of the rotor by electrically conducting end-rings, thus producing a conducting cage-like structure, as shown in Fig. 11-17b. Such a rotor, called a squirrel-cage rotor, has a low cost, and rugged nature.

11-6-2 Principles of Induction Motor Operation

Figure 11-18a shows the stator windings whose voltages are shown in the phasor diagram of Fig. 11-18b, where the frequency of the applied line-voltages to the motor is f in Hz, and V_{rms} is the magnitude in rms

$$\overline{V}_a = V_{rms} \angle 0^o, \quad \overline{V}_b = V_{rms} \angle -120^o, \text{ and } \quad \overline{V}_c = V_{rms} \angle -240^o \tag{11-27}$$

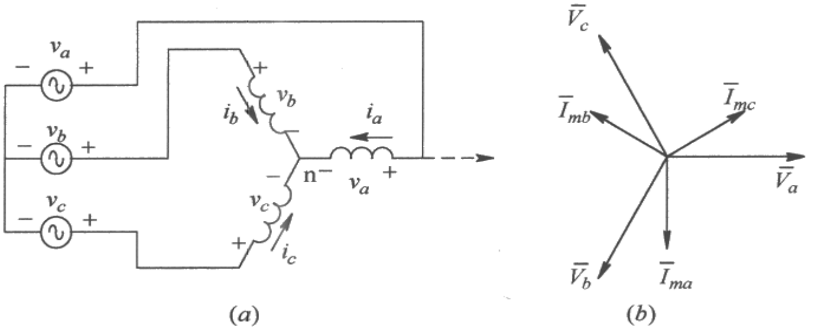


Figure 11-18 Induction machine: applied voltages and magnetizing currents.

By Faraday's law, the applied stator voltages given in Eq. 11-27 establish a rotating flux-density distribution in the air gap by drawing magnetizing currents of rms value I_m, which are shown in Fig. 11-18b:

$$\overline{I}_{ma} = \text{I}_m \angle -90^o, \quad \overline{I}_{mb} = \text{I}_m \angle -210^o, \text{ and } \quad \overline{I}_{mc} = \text{I}_m \angle -330^o \tag{11-28}$$

As these currents vary sinusoidally with time, the combined flux-density distribution in the air gap produced by these currents rotates at a synchronous speed ω_{syn}, where

$$\omega_{syn} = 2\pi f \qquad \left(\omega_{syn} = \frac{2\pi f}{p/2} \quad \text{for a } p\text{-pole machine} \right) \tag{11-29}$$

The rotor in an induction motor turns (due to the electromagnetic torque developed, as will be discussed shortly) at a speed ω_m in the same direction as the rotation of the air gap flux-density distribution, such that $\omega_m < \omega_{syn}$. Therefore, there is a relative speed between the flux-density distribution rotating at ω_{syn} and the rotor conductors at ω_m. This relative speed, that is the speed at which the rotor is "slipping" with respect to the rotating flux-density distribution, is called the slip speed:

$$\textit{slip speed} \quad \omega_{slip} = \omega_{syn} - \omega_m \tag{11-30}$$

By Faraday's Law $(e = B\ell u)$, voltages are induced in the rotor bars at the slip frequency due to the relative motion between the flux-density distribution and the rotor, where the slip frequency f_{slip} in terms of the frequency f of the stator voltages and currents is

$$\textit{slip frequency} \qquad f_{slip} = \frac{\omega_{slip}}{\omega_{syn}} f \qquad (11\text{-}31)$$

Since the rotor bars are shorted at both ends, these induced bar voltages cause slip-frequency currents to flow in the rotor bars. The rotor-bar currents interact with the flux-density distribution established by the stator-applied voltages, and the result is a net electromagnetic torque T_{em} in the same direction as the rotor's rotation.

The sequence of events in an induction machine to meet the load torque demand is as follows: At essentially no load, an induction machine operates nearly at the synchronous speed that depends on the frequency of applied stator voltages (Eq. 11-29). As the load toque increases, the motor slows down, resulting in a higher value of slip speed. Higher slip speed results in higher voltages induced in the rotor bars and hence higher rotor-bar currents. Higher rotor-bar currents result in a higher electromagnetic torque to satisfy the increased load-torque demand.

Neglecting second-order effects, the air gap flux is totally determined by the applied stator voltages. Hence, the air gap flux produced by the rotor-bar currents is nullified by the additional currents drawn by the stator windings, which are in addition to the magnetizing currents in Eq. 11-28.

11-6-3 Per-Phase Equivalent Circuit of Induction Machines

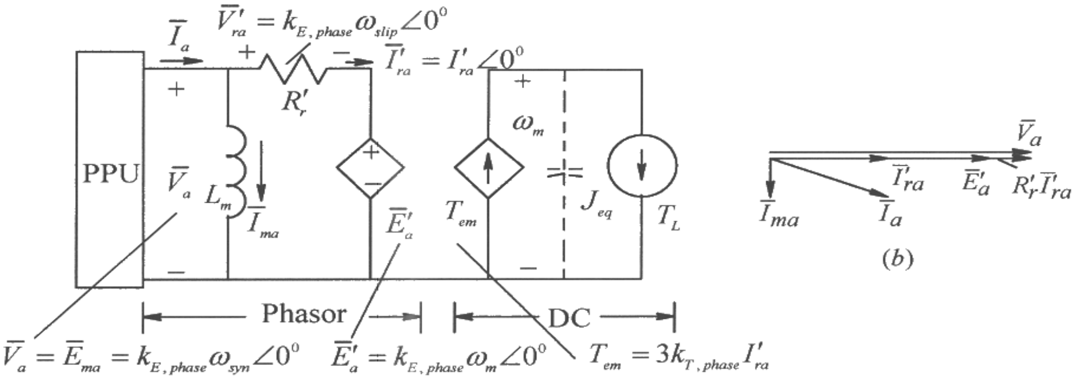
In this balanced three-phase sinusoidal steady state analysis, we will neglect second-order effects such as the stator winding resistance and leakage inductance, and the rotor circuit leakage inductance. As shown in Fig. 11-19a for phase-a in this per-phase circuit, $\overline{V}_a$ and so on are applied at a frequency f, which results in magnetizing currents to establish the air gap flux-density distribution in the air gap, represented as flowing through a magnetizing inductance L_m. The voltage magnitude and frequency are such that the magnitude of the flux-density distribution in the air gap is at its rated value and this distribution rotates counter-clockwise at the desired ω_{syn} (Eq. 11-29) to induce a back-emf in the stationary stator phase windings such that

$$\overline{V}_a = \overline{E}_{ma} = k_{E,phase}\,\omega_{syn}\angle 0^0 \qquad (11\text{-}32)$$

where, $k_{E,phase}$ is the machine per-phase voltage-constant.

Next, we will consider the effect of the rotor-bar currents. The rotor-bar currents result in additional stator currents (in addition to the magnetizing current), which can be represented on a per-phase basis by a current $\overline{I}'_{ra}$ in-phase with the applied voltage (since the rotor-circuit leakage inductance is ignored), as shown in Fig. 11-19a

$$\overline{I}'_{ra} = I'_{ra}\angle 0^0 \tag{11-33}$$



$\overline{V}'_{ra} = k_{E,phase}\omega_{slip}\angle 0^0$
$\overline{I}_a$
$\overline{I}'_{ra} = I'_{ra}\angle 0^0$
R'_r
PPU
$\overline{V}_a$
L_m
$\overline{I}_{ma}$
$\overline{E}'_a$
T_{em}
ω_m
J_{eq}
T_L
Phasor
DC
$\overline{V}_a = \overline{E}_{ma} = k_{E,phase}\omega_{syn}\angle 0^0$
$\overline{E}'_a = k_{E,phase}\omega_m\angle 0^0$
$T_{em} = 3k_{T,phase}I'_{ra}$
$\overline{V}_a$
$\overline{I}_{ra}$
$\overline{E}'_a$
$R'_r\overline{I}_{ra}$
$\overline{I}_{ma}$
$\overline{I}_a$
(b)

(a)

Figure 11-19 Induction motor equivalent circuit and phasor diagram.

The flux-density distribution (although produced differently than in PMAC machines) interacts with these stator currents, just like in PMAC machines, and hence the per-phase torque-constant equals the per-phase voltage constant

$$k_{T,phase} = k_{E,phase} \tag{11-34}$$

The per-phase torque can be expressed as

$$T_{em,phase} = k_{T,phase}I'_{ra} \tag{11-35}$$

This torque at a mechanical speed ω_m results in per-phase electromagnetic power that gets converted to mechanical power, where using Eqs. 11-34 and 11-35

$$P_{em,phase} = \omega_m T_{em,phase} = \omega_m k_{E,phase} I'_{ra} \tag{11-36}$$

In Eq. 11-36, $\left(\omega_m k_{E,phase}\right)$ can be considered the back-emf $\overline{E}'_a$, just like in the DC and the PMAC machines, as shown in Fig. 11-19a

$$\overline{E}'_a = \omega_m k_{E,phase}\angle 0^0 \tag{11-37}$$

In the rotor-circuit, the voltages induced depend on the slip-speed ω_{slip}, and overcome the *IR* voltage drop in the rotor bar resistances. The rotor-bar resistances, and the voltage drop and the power losses in them, are represented in the per-phase equivalent circuit of

Fig. 11-19a by a voltage drop across an equivalent resistance R'_r. Using the Kirchhoff's voltage law in Fig. 11-19a,

$$\bar{V}'_{ra} = \underbrace{k_{E,phase}\omega_{syn}\angle 0^0}_{\bar{E}_{ma}} - \underbrace{k_{E,phase}\omega_m\angle 0^0}_{\bar{E}'_a} = k_{E,phase}\omega_{slip}\angle 0^0 \qquad (11\text{-}38)$$

Hence,

$$I'_{ra} = \left(\frac{k_{E,phase}}{R'_r}\right)\omega_{slip} \qquad (11\text{-}39)$$

Using Eqs. 11-34, 11-36 and 11-39, the combined torque of all three phases is

$$T_{em} = \frac{P_{em}}{\omega_m} = \underbrace{\left(3\frac{k^2_{T,phase}}{R'_r}\right)}_{k_{T,\omega_{slip}}}\omega_{slip} \qquad (11\text{-}40)$$

where $k_{T,\omega_{slip}}$ in the above equation is a machine constant that shows that the torque produced is linearly proportional to the slip speed. Using Eqs. 11-30 and 11-40,

$$\omega_m = \omega_{syn} - \frac{T_{em}}{k_{T,\omega_{slip}}} \qquad (11\text{-}41)$$

Based on Eq. 11-41, the torque-speed characteristics are shown in Fig. 11-20a for various applied frequencies to the stator. The stator voltage as function of frequency is shown in Fig. 11-20b to maintain the peak of the flux-density distribution at its rated value. The relationship between the voltage and the synchronous speed or f shown in Fig. 11-20b is approximate. It needs a substantially higher voltage than indicated (shown dotted) at very low frequencies where the voltage drop across the stator winding resistance R_s becomes substantial at higher torque loading, and hence cannot be neglected.

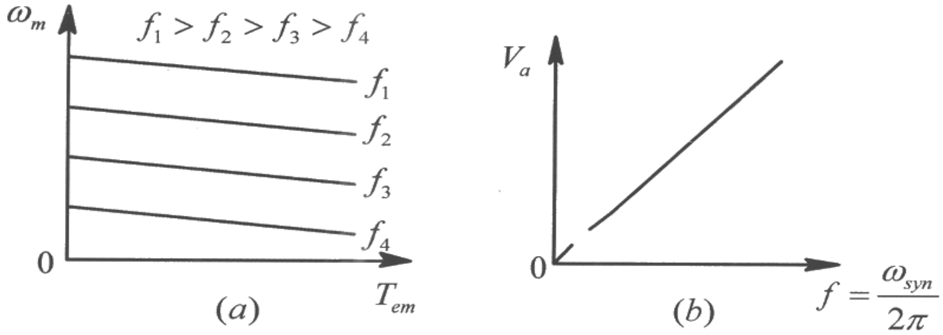


Figure 11-20 Induction motors: Torque-speed characteristics and voltage vs. frequency.

11-7 SUMMARY

The discussion above shows the requirements of three common types of machines supplied through power-electronics based power processing units in steady state.

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1. N. Mohan, *Electric Drives: An Integrative Approach*, year 2003 Edition, MNPERE, Minneapolis, www.MNPERE.com.
2. N. Mohan, Advanced *Electric Drives: Analysis, Modeling and Simulation using Simulink*, year 2001 Edition, MNPERE, Minneapolis, www.MNPERE.com.

PROBLEMS

Mechanical Systems

11-1 A constant torque of 5 *Nm* is applied to an unloaded motor at rest at time $t = 0$. The motor reaches a speed of 1800 *rpm* in 4 *s*. Assuming the damping to be negligible, calculate the motor inertia.

11-2 In an electric-motor drive similar to that shown in Fig. 11-2a, the combined inertia is $J_{eq} = 5 \times 10^{-3} kg \cdot m^2$. The load torque is $T_L = 0.05 kg \cdot m^2$. Draw the electrical equivalent circuit and plot the electromagnetic torque required from the motor to bring the system linearly from rest to a speed of 100 rad/s in 4 s, and then to maintain that speed.

11-3 Plot the power required in Problem 11-2.

DC Motors

11-4 A permanent-magnet dc motor has the following parameters: $R_a = 0.35\Omega$ and $k_E = k_T = 0.5$ in MKS units. For a torque of up to 8 *Nm*, plot its steady state torque-speed characteristics for the following values of V_a: 100V, 75V, and 50V.

11-5 Consider the dc motor of Problem 11-4 whose moment-of-inertia $J_m = 0.02 kg \cdot m^2$. Its armature inductance L_a can be neglected for slow changes. The motor is driving a load of inertia $J_L = 0.04 kg \cdot m^2$. The steady state operating speed is 300 *rad/s*. Calculate and plot the terminal voltage $v_a(t)$ that is required to bring this motor to a halt as quickly as possible, without exceeding the armature current of 12 A.

Permanent-Magnet AC Motors

11-6 In a three-phase, 2-pole, brushless-dc motor, the torque constant $k_T = 0.5 Nm/A$. Calculate the phase currents if the motor is to produce a counter-clockwise torque of $5 Nm$.

11-7 In a 2-pole, three-phase (PMAC) brushless-dc motor drive, the torque constant k_T and the voltage constant k_E are 0.5 in *MKS* units. The synchronous inductance is *15 mH* (neglect the winding resistance). This motor is supplying a torque of *3 Nm* at a speed of *3,000* rpm in a balanced sinusoidal steady state. Calculate the per-phase voltage across the power-processing unit as it supplies controlled currents to this motor.

Induction Motors

11-8 Consider an induction machine that has 2 poles and is supplied by a rated voltage of 208 *V* (line-to-line, rms) at the frequency of 60 *Hz*. It is operating in steady state and is loaded to its rated torque. Neglect the stator leakage impedance and the rotor leakage flux. The per-phase magnetizing current is 4.0 *A* (rms). The current drawn per-phase is 10 *A* (rms) and is at an angle of 23.56 degrees (lagging). Calculate the per-phase current if the mechanical load decreases so that the slip speed is one-half that of the rated case.

11-9 In Problem 11-8, the rated speed (while the motor supplies its rated torque) is 3475 rpm. Calculate the slip speed ω_{slip}, and the slip frequency f_{slip} of the currents and voltages in the rotor circuit.

11-10 In Problem 11-9, the rated torque supplied by the motor is 8 *Nm*. Calculate the torque constant, which linearly relates the torque developed by the motor to the slip speed.

11-11 A three-phase, 60-*Hz*, 4-pole, 440-*V* (line-line, rms) induction-motor drive has a full-load (rated) speed of 1746 *rpm*. The rated torque is 40 *Nm*. Keeping the air gap flux-density peak constant at its rated value, (a) plot the torque-speed characteristics (the linear portion) for the following values of the frequency f : 60 *Hz*, 45 *Hz*, 30 *Hz*, and 15 *Hz*. (b) This motor is supplying a load whose torque demand increases linearly with speed, such that it equals the rated torque of the motor at the rated motor speed. Calculate the speeds of operation at the four values of frequency in part (a).

11-12 In the motor drive of Problem 11-11, the induction motor is such that while applied the rated voltages and loaded to the rated torque, it draws 10.39 A (rms) per-phase at a power factor of 0.866 (lagging). $R_s = 1.5\Omega$. Calculate the voltages corresponding to the four values of the frequency f to maintain $\hat{B}_{ms} = \hat{B}_{ms,rated}$.

Chapter 12

SYNTHESIS OF DC AND LOW-FREQUENCY SINUSOIDAL AC VOLTAGES FOR MOTOR DRIVES AND UPS

12-1 INTRODUCTION

Motor drives (ac and dc) are important application areas of power electronics with market value of tens of billions dollars annually, as described in Chapter 1. Uninterruptible power supplies (UPS) are a special case of ac motor drives in discussing the role of power electronics, and will be briefly discussed in section 12-6 in this chapter.

In motor drive applications, the voltage-link structure of Fig. 1-16, repeated in Fig. 12-1, is used, where our emphasis will be to discuss how the load-side converter with the dc voltage as an input synthesizes dc or low-frequency sinusoidal voltage outputs. Functionally, this converter operates as a linear amplifier, amplifying a control signal, dc in case of dc-motor drives, and ac in case of ac-motor drives. The power flow through this converter should be reversible.

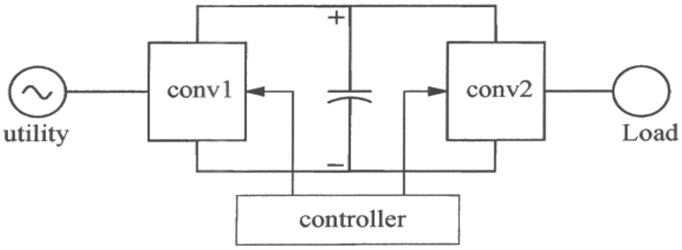


Figure 12-1 Voltage-link system.

These converters consist of bi-directional switching power-poles discussed earlier, two in case of dc-motor drives and three in ac motor drives, as shown in Figs. 12-2a and b.

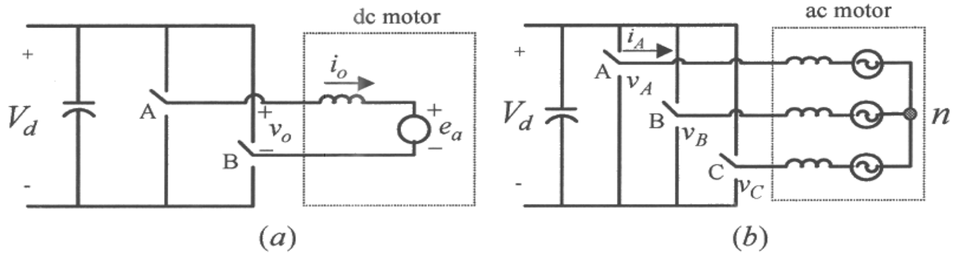


Figure 12-2 Converters for dc and ac motor drives.

12-2 SWITCHING POWER-POLE AS THE BUILDING BLOCK

To synthesize dc or low-frequency sinusoidal ac outputs, these converters consist of the switching power-pole shown in Fig. 12-3a with the bi-directional current capability, which was introduced in Chapter 3. It consists of a parallel combination of Buck and Boost converters, as shown in Fig. 12-3b, where the two transistors are controlled by complimentary gate signals. This implementation and the complimentary gating of transistors allow a continuous bi-directional power and current capability as discussed below, and hence ideally a discontinuous conduction mode does not exist. The average representation by an ideal transformer is shown in Fig. 12-3c.

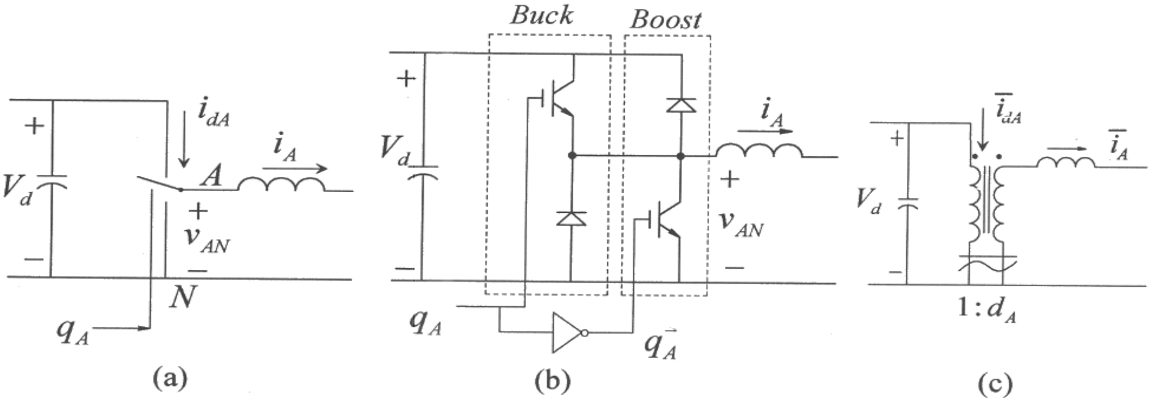


Figure 12-3 Bi-directional switching power-pole.

12-2-1 Pulse-Width-Modulation (PWM) of the Bi-Directional Switching Power-Pole

It is clear from the discussion of the switching power-poles that the output voltages of these poles at the current-port are always of a positive polarity. However, the output voltages of converters for motor drives must be reversible in polarity. This is achieved as shown in Fig. 12-2 by the differential output between two switching power-poles in dc-motor drives, and between any two of the three power-poles in ac motor drives.

The average representation of a switching power-pole is shown in Fig. 12-4a. In each switching pole, the output voltage at the current-port includes a dc offset of $V_d/2$ (that corresponds to the duty-ratio d_A equal to 0.5). To synthesize a low-frequency sine wave, for example, varying the duty-ratio sinusoidally around 0.5, the average output voltage varies sinusoidally around $V_d/2$, as shown in Fig. 12-4b. The average output voltage can range from 0 and V_d. In the differential output between two power-poles in converters for dc drives, and between any two of the three poles for ac drives, shown in Fig. 12-2a and b, the dc offset is neutralized as will be discussed in the following sections in this chapter.

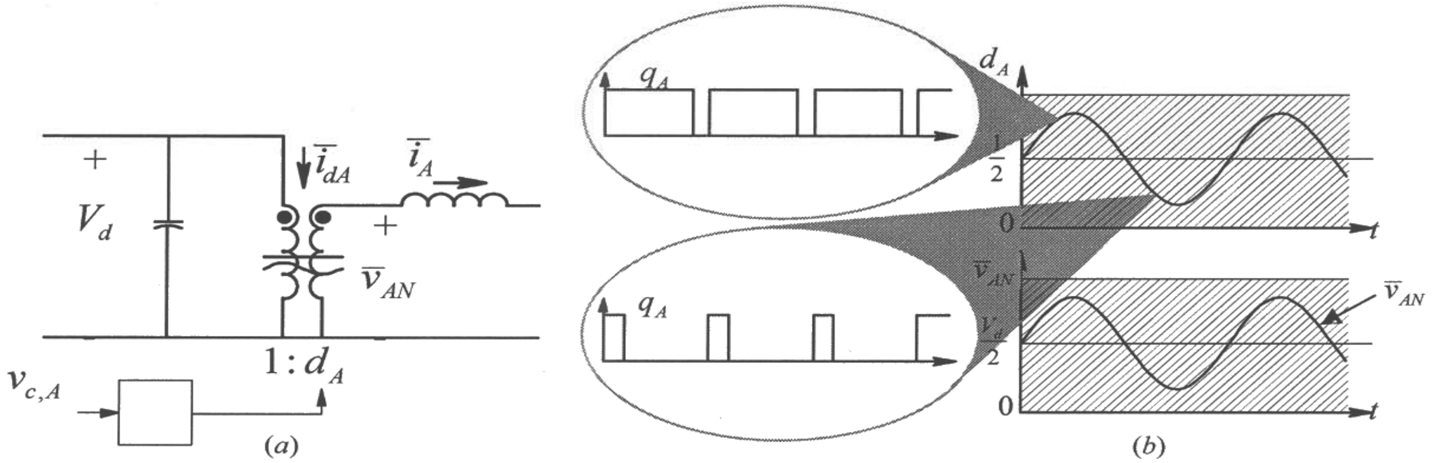

+
V_d
$\bar{i}_{dA}$
$\bar{i}_A$
+
$\bar{v}_{AN}$
$1:d_A$
$v_{c,A}$
(a)
q_A
q_A
d_A
$\frac{1}{2}$
0
t
$\bar{v}_{AN}$
$\frac{V_d}{2}$
0
t
$\bar{v}_{AN}$
(b)

Figure 12-4 Varying the duty-ratio around 0.5 varies $\bar{v}_{AN}$ around $V_d/2$.

In motor drives, to generate the switching function q_A, a triangular-waveform signal v_{tri} is used for comparison in the PWM-IC, as shown in Fig. 12-5a, where the peak value $\hat{V}_{tri}$ is kept constant and the frequency of the triangular waveform establishes the switching frequency f_s.

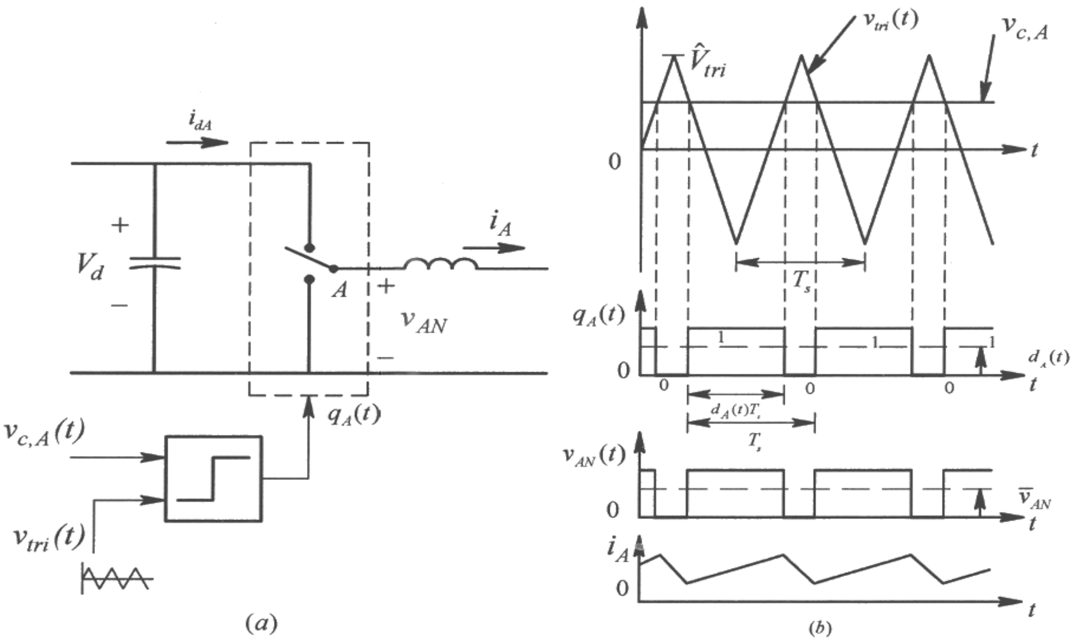

i_{dA}
+
V_d
−
A
+
v_{AN}
−
i_A
$q_A(t)$
$v_{c,A}(t)$
$v_{tri}(t)$
(a)
$v_{tri}(t)$
$v_{c,A}$
$\hat{V}_{tri}$
0
t
T_s
$q_A(t)$
1
1
1
0
0
0
0
$d_A(t)$
t
$d_A(t)T_s$
T_s
$v_{AN}(t)$
0
$\bar{v}_{AN}$
t
i_A
0
t
(b)

Figure 12-5 Switching power-pole and its voltage and current waveforms.

The resulting switching-signal waveforms are shown in Fig. 12-5b. The duty-ratio d_A, obtained by comparison of these linear waveforms, can be derived by considering two values of the control signal $v_{c,A}$: $\hat{V}_{tri}$ results in d_A to equal 1, and $(-\hat{V}_{tri})$ results in d_A to equal 0. Linearly interpolating between these two values, the expression for d_A can be written as

$$d_A(t) = 0.5 + 0.5\frac{v_{c,A}(t)}{\hat{V}_{tri}} \qquad (0 < d_A < 1) \qquad (12\text{-}1)$$

which shows that it consists of two terms – a dc offset of 0.5 and a term that is linearly proportional to the control voltage $v_{c,A}(t)$. Therefore, the average output voltage of the power-pole can be written as

$$\bar{v}_{AN}(t) = d_A(t)V_d = \underbrace{0.5V_d}_{dc\,offset} + \underbrace{0.5\frac{V_d}{\hat{V}_{tri}}}_{k_{pole}} v_{c,A}(t) \qquad (12\text{-}2)$$

where $0.5V_d$ is the dc offset and k_{pole} is the gain by which the control signal is amplified to produce the output voltage. The average representation of the pulse-width-modulated switching power-pole is shown Fig. 12-6.

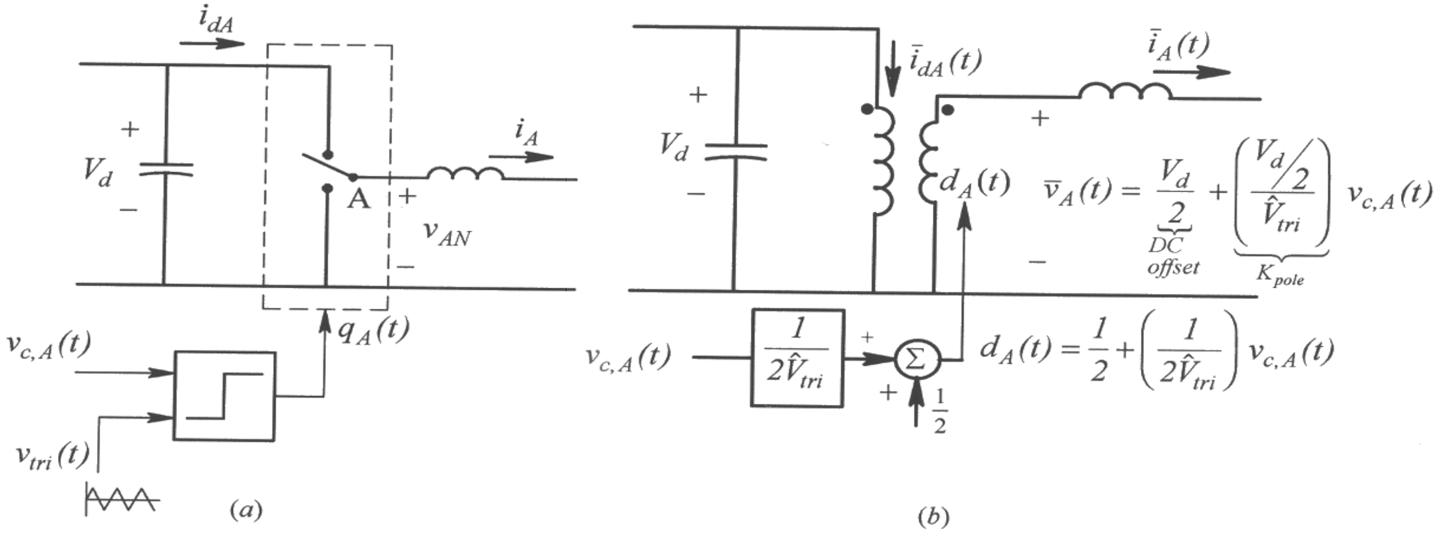

i_{dA}
i_A
+
V_d
−
A
+
v_{AN}
−
$q_A(t)$
$v_{c,A}(t)$
$v_{tri}(t)$
(a)
$\bar{i}_{dA}(t)$
$\bar{i}_A(t)$
+
V_d
−
$d_A(t)$
+
$\bar{v}_A(t) = \underbrace{\frac{V_d}{2}}_{DC\ offset} + \underbrace{\left(\frac{V_d/2}{\hat{V}_{tri}}\right)}_{K_{pole}} v_{c,A}(t)$
−
$v_{c,A}(t)$
$\frac{1}{2\hat{V}_{tri}}$
+
Σ
+
$\frac{1}{2}$
$d_A(t) = \frac{1}{2} + \left(\frac{1}{2\hat{V}_{tri}}\right) v_{c,A}(t)$
(b)

Figure 12-6 Average representation of the pulse-width-modulated power-pole.

12-2-3 Harmonics in the PWM Waveforms v_A and i_{dA}

Although only their average values are of interest, we must recognize that the voltage v_A and the current i_{dA} contain harmonics in addition to their intended average values. Fourier analysis of these waveforms shows that they contain components at frequencies at the multiples of the switching frequency f_s, with sidebands located at the multiples of the frequency f_1 being synthesized by the switching power-pole. These harmonic frequencies can be expressed as follows, where k_1 and k_2 are constants, which can take on values 1, 2, 3, and so on:

$$f_h = k_1 f_s \pm \underbrace{k_2 f_1}_{\text{sidebands}} \qquad (12\text{-}3)$$

This harmonic analysis is graphically shown in Fig. 12-7, which highlights the importance of selecting a high switching frequency. Clearly, the harmonic components in v_A at frequencies f_h given by Eq. 12-3 are undesirable but also unavoidable in a switching power-pole. However, the minimum value in f_h depends on f_s, and by selecting a high switching frequency, all the harmonic frequencies are pushed to the correspondingly high values. At these high values, the series inductance at the current-port becomes very effective in ensuring that the current i_A has a small ripple in spite of the pulsating v_A. Similarly, the high-frequency components in i_{dA} are filtered by a relatively small capacitor across the voltage-port. For this reason in modern power electronic systems, it is typical to use switching frequencies a few hundred kHz in dc-dc converters at low power, and a few tens of kHz in converters for motor drives up to a few hundred kW.

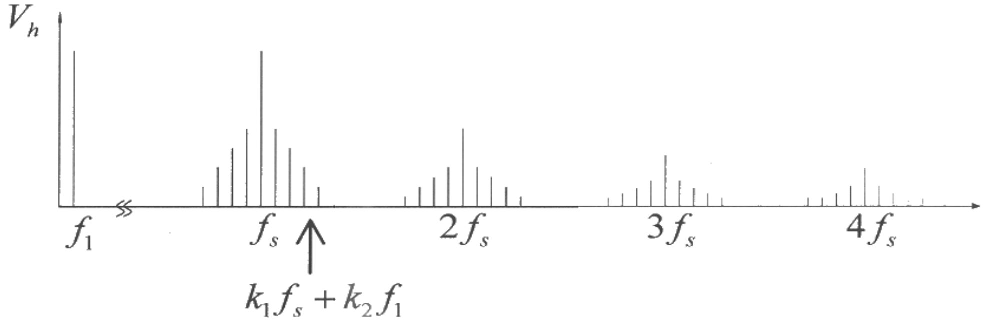
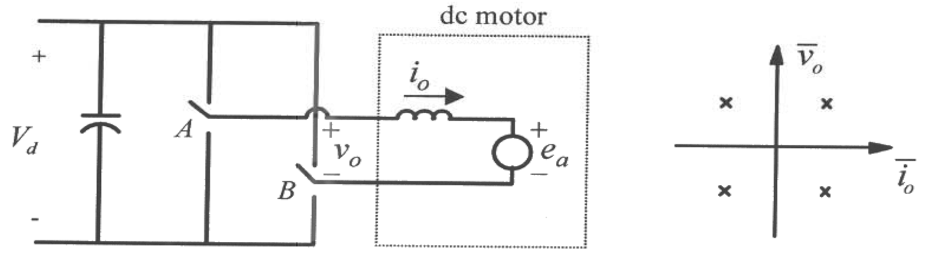


Figure 12-7 Harmonics in the switching power-pole.

12-3 DC-MOTOR DRIVES

In dc-motor drives as shown by Fig. 12-8a, the dc motor is controlled by the dc voltage v_o applied to its terminals. The converter consists of two bi-directional switching power-poles, which are pulse-width-modulated. Allowing the power (and hence the current) through this converter to be bi-directional facilitates the machine to operate both in motor and as well in its generator mode, in either direction of rotation, as shown in Fig. 12-8b in terms of average terminal quantities. Motoring-mode in the forward direction rotation is represented by quadrant 1 with positive voltage and current. While rotating in the forward direction, this machine can be slowed down by making the machine go into its generator mode in which the power flow reverses, as shown by quadrant 2 with a positive voltage and a negative current. Motoring in the reverse direction of rotation requires voltage and current both negative, corresponding to quadrant 3. While rotating in the reverse direction, the generator-mode in quadrant 4 slows down the machine.



(*a*) (*b*)

Figure 12-8 DC-motor four-quadrant operation.

In dc-motor drives, as shown in Fig. 12-9a, the control voltage $v_c(t)$ produced by the feedback controller is applied as $v_{c,A}(t)$, equal to $v_c(t)$, to produce the switching function $q_A(t)$ for pole-*A*. The control voltage for pole-*B* is negative of the control voltage for pole-*A*: $v_{c,B}(t) = -v_c(t)$. The average representation of the two poles is shown in Fig. 12-9b and the switching waveforms are shown in Fig. 12-9c. Using Eq. 12-1

$$\overline{v}_{AN}(t) = d_A(t)V_d = 0.5V_d + 0.5\frac{V_d}{\hat{V}_{tri}}v_c(t) \qquad (12\text{-}4)$$

$$\overline{v}_{BN}(t) = d_B(t)V_d = 0.5V_d - 0.5\frac{V_d}{\hat{V}_{tri}}v_c(t) \qquad (12\text{-}5)$$

$$\overline{v}_o(t) = \overline{v}_{AN}(t) - \overline{v}_{BN}(t) = \underbrace{\frac{V_d}{\hat{V}_{tri}}}_{k_{pwm}}v_c(t) \qquad (12\text{-}6)$$

where k_{pwm} is the gain by which the control voltage is amplified by this switch-mode converter to apply the voltage at the terminals of this dc machine. This output voltage can be controlled in a range from $(-V_d)$ to V_d. Thus, a four-quadrant converter is realized by using two-poles, each of which is capable of a two-quadrant operation.

The total average dc-side current is the sum of the average dc-side currents of each pole in Fig. 12-9b:

$$\overline{i}_d(t) = \overline{i}_{dA} + \overline{i}_{dB} = d_A(t)\overline{i}_A(t) + d_B(t)\overline{i}_B(t) \qquad (12\text{-}7)$$

Using the values of the duty-ratios of the two poles, and recognizing the directions with which the currents are defined,

$$i_A(t) = -i_B(t) = i_o(t) \qquad (12\text{-}8)$$

Thus, using Eq. 12-1 to achieve d_A and d_B in terms of $v_c(t)$ and substituting them in Eq. 12-7 along with the currents from Eq. 12-8:

$$\bar{i}_d(t) = \frac{v_c(t)}{\hat{V}_{tri}}\bar{i}_o(t) \tag{12-9}$$

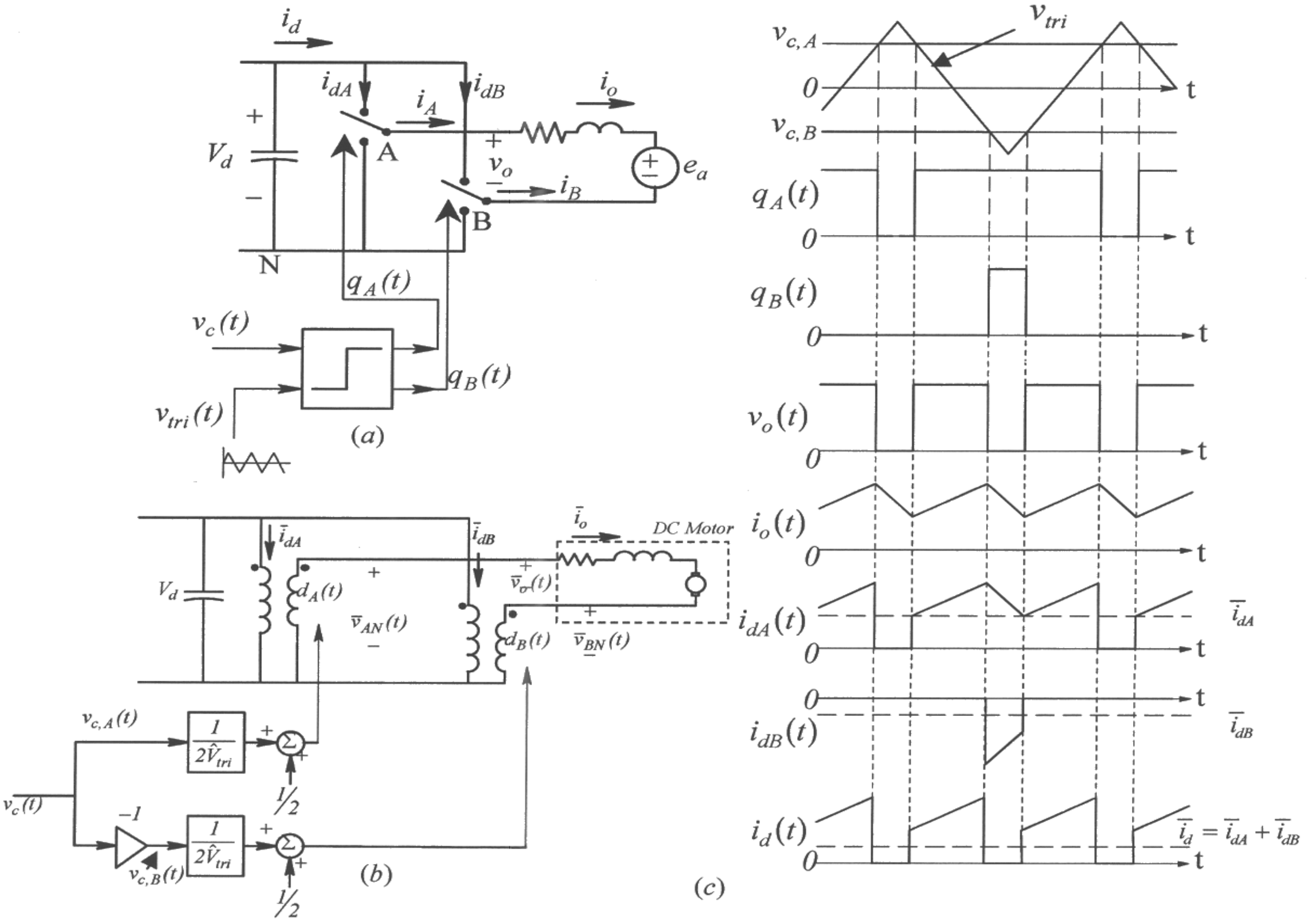

i_d
i_{dA}
i_{dB}
i_A
i_o
V_d
+
−
A
B
N
v_o
i_B
e_a
$q_A(t)$
$v_c(t)$
$q_B(t)$
$v_{tri}(t)$
(a)
$\bar{i}_{dA}$
$\bar{i}_{dB}$
$\bar{i}_o$
DC Motor
V_d
$d_A(t)$
$\bar{v}_{AN}(t)$
$\bar{v}_o(t)$
$d_B(t)$
$\bar{v}_{BN}(t)$
$v_{c,A}(t)$
$\frac{1}{2\hat{V}_{tri}}$
Σ
½
$v_c(t)$
−1
$v_{c,B}(t)$
(b)
v_{tri}
$v_{c,A}$
0
t
$v_{c,B}$
$q_A(t)$
$q_B(t)$
$v_o(t)$
$i_o(t)$
$i_{dA}(t)$
$\bar{i}_{dA}$
$i_{dB}(t)$
$\bar{i}_{dB}$
$i_d(t)$
$\bar{i}_d = \bar{i}_{dA} + \bar{i}_{dB}$
(c)

Figure 12-9 Converter for dc-motor drives.

The instantaneous quantities associated with this switch-mode dc-dc converter are pulsating, as shown in Fig. 12-9c. Based on the discussion of harmonic components in the voltage at the current-port and in the current at the voltage-port of each power-pole, we can calculate cancellation of some harmonics in the combination of the two power-poles in a dc-drive converter. A detailed discussion of this can be found in reference [1].

12-4 AC-MOTOR DRIVES

Ac-motor drives are the workhorse of industry. These three-phase motors are controlled in speed and position by applying adjustable-magnitude, and adjustable-frequency ac voltages by three bi-directional switching power-poles, as shown in Fig. 12-10a. Their average representation is shown in Fig. 12-10b.

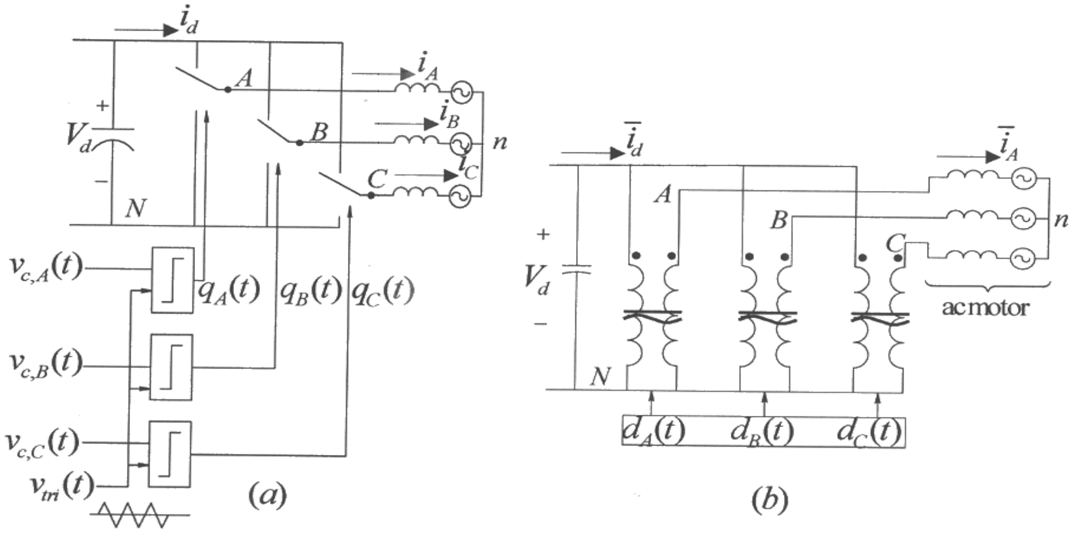


Figure 12-10 Converter for three-phase motor drive and UPS.

In order to synthesize balanced three-phase voltages, the PWM signals for the switches in Fig. 12-10a are obtained by comparing three control signals, which establish the amplitude and the frequency of the output voltages, with a triangular waveform v_{tri}, as shown in Fig. 12-11

$$\begin{aligned} v_{c,A}(t) &= \hat{V}_c \sin \omega_1 t \\ v_{c,B}(t) &= \hat{V}_c \sin(\omega_1 t - 120^o) \\ v_{c,C}(t) &= \hat{V}_c \sin(\omega_1 t - 240^o) \end{aligned} \tag{12-10}$$

The resulting voltage waveforms are shown in Fig. 12-11. Using Eq. 12-10 into equations similar to Eq. 12-1 for all three phases produces the following duty-ratios in the average representation shown in Fig. 12-10b, where the control voltages and the duty-ratios are plotted in Fig. 12-12:

$$\begin{aligned} d_A(t) &= 0.5 + \frac{\hat{V}_c}{\hat{V}_{tri}} \sin \omega_1 t \\ d_B(t) &= 0.5 + \frac{\hat{V}_c}{\hat{V}_{tri}} \sin(\omega_1 t - 120^o) \\ d_C(t) &= 0.5 + \frac{\hat{V}_c}{\hat{V}_{tri}} \sin(\omega_1 t - 240^o) \end{aligned} \tag{12-11}$$

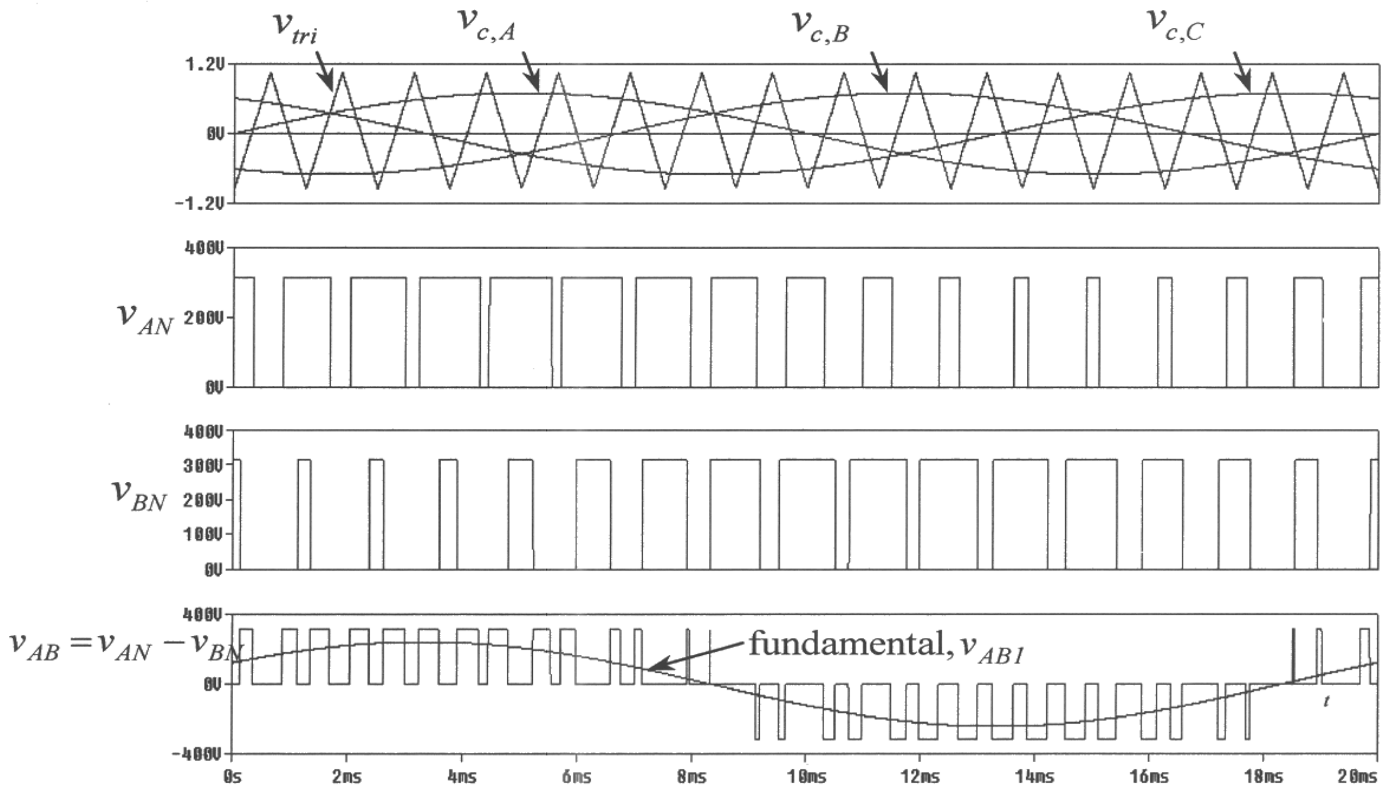


Figure 12-11 Switching waveforms in three-phase converter.

Applying the duty-ratios in Eq. 12-11 in Fig. 12-10b results in the following average output voltages:

$$
\begin{aligned}
\bar{v}_{AN}(t) &= 0.5V_d + \underbrace{0.5\frac{V_d}{\hat{V}_{tri}}}_{k_{pole}} \underbrace{\hat{V}_c \sin \omega_1 t}_{v_{c,A}} \\
\bar{v}_{BN}(t) &= 0.5V_d + \underbrace{0.5\frac{V_d}{\hat{V}_{tri}}}_{k_{pole}} \underbrace{\hat{V}_c \sin(\omega_1 t - 120^o)}_{v_{c,B}} \\
\bar{v}_{CN}(t) &= 0.5V_d + \underbrace{0.5\frac{V_d}{\hat{V}_{tri}}}_{k_{pole}} \underbrace{\hat{V}_c \sin(\omega_1 t - 240^o)}_{v_{c,C}}
\end{aligned}
\qquad (12\text{-}12)
$$

where the pole gain k_{pole} is the same as in Eq. 12-2, and it amplifies the control voltage for each switching power-pole. These voltages are plotted in Fig. 12-12. The average output voltages of the switching power-poles have the same offset voltage, equal to $0.5V_d$. These equal offset voltages in each phase are considered zero-sequence voltages, which cannot cause any current to flow when applied to a balanced three-phase motor load shown in Fig. 12-10a or b.

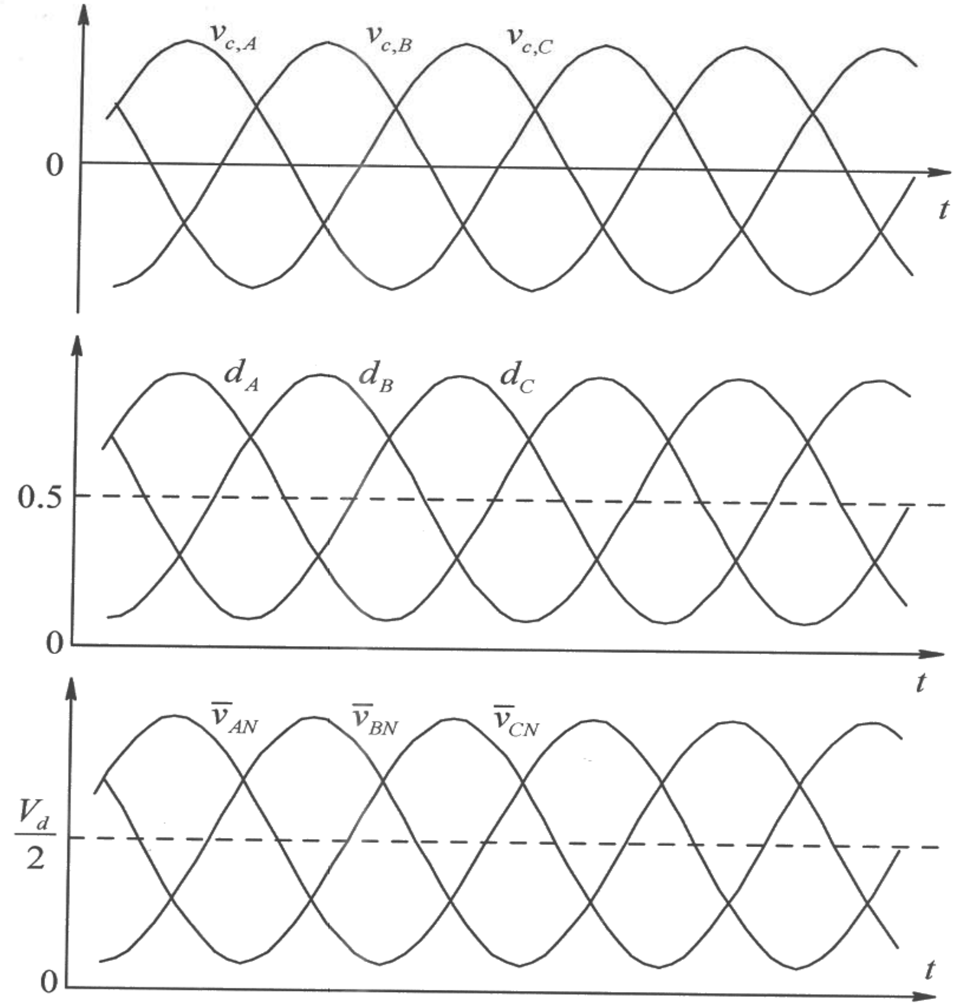


Figure 12-12 Duty-ratios and the average output voltages of the power-pole.

Hence the dc component in each phase voltage (terminal to neutral *n*) of the motor load equals zero. As a consequence in Fig. 12-10b, the average phase-neutral voltages across the motor phases, with respect to the motor neutral *n*, are as intended

$$\begin{aligned}
\overline{v}_{An}(t) &= \left(0.5\frac{V_d}{\hat{V}_{tri}}\right)\hat{V}_c \sin\omega_1 t \\
\overline{v}_{Bn}(t) &= \left(0.5\frac{V_d}{\hat{V}_{tri}}\right)\hat{V}_c \sin(\omega_1 t - 120^o) \qquad (12\text{-}13) \\
\overline{v}_{Cn}(t) &= \left(0.5\frac{V_d}{\hat{V}_{tri}}\right)\hat{V}_c \sin(\omega_1 t - 240^o)
\end{aligned}$$

where the amplitude of these phase voltages are

$$\hat{V} = \left(\frac{\hat{V}_c}{\hat{V}_{tri}}\right)\frac{V_d}{2} \qquad (12\text{-}14)$$

We should note that at high switching frequency f_s relative to the fundamental frequency f_1 being synthesized, average voltages in Eq. 12-13 equal the fundamental-frequency components (v_{An1}, v_{Bn1}, v_{Cn1}) in the voltages applied to the motor phases (at the terminals with respect to the motor-neutral *n*).

To obtain the average currents drawn from the voltage-port of each switching power-pole, we will assume the average currents drawn by the motor load in Fig. 12-10b to be sinusoidal but lagging with respect to the average voltages in each phase by an angle ϕ_1,

$$\begin{aligned}\bar{i}_A(t) &= \hat{I}\sin(\omega_1 t - \phi_1)\\ \bar{i}_B(t) &= \hat{I}\sin(\omega_1 t - \phi_1 - 120^o)\\ \bar{i}_C(t) &= \hat{I}\sin(\omega_1 t - \phi_1 - 240^o)\end{aligned} \tag{12-15}$$

Therefore in Fig. 12-10b, the average currents drawn from the voltage-port are

$$\begin{aligned}\bar{i}_{dA}(t) &= d_A(t)\,\bar{i}_A(t) = 0.5\,\bar{i}_A(t) + 0.5\frac{v_{c,A}(t)}{\hat{V}_{tri}}\,\bar{i}_A(t)\\ \bar{i}_{dB}(t) &= d_B(t)\,\bar{i}_B(t) = 0.5\,\bar{i}_B(t) + 0.5\frac{v_{c,B}(t)}{\hat{V}_{tri}}\,\bar{i}_B(t)\\ \bar{i}_{dC}(t) &= d_C(t)\,\bar{i}_C(t) = 0.5\,\bar{i}_C(t) + 0.5\frac{v_{c,C}(t)}{\hat{V}_{tri}}\,\bar{i}_C(t)\end{aligned} \tag{12-16}$$

The total average current drawn by the converter from the dc-side voltage source is the sum of the three currents above:

$$\bar{i}_d(t) = \bar{i}_{dA}(t) + \bar{i}_{dB}(t) + \bar{i}_{dC}(t) \tag{12-17}$$

In Eq. 12-15, applying Kirchoff's law to average currents at the motor-neutral, the sum of three average currents equals zero,

$$\bar{i}_A(t) + \bar{i}_B(t) + \bar{i}_C(t) = 0 \tag{12-18}$$

Therefore, substituting Eqs. 12-16 and making use of Eq. 12-18 in Eq. 12-17

$$\bar{i}_d(t) = \frac{0.5}{\hat{V}_{tri}}\left[v_{c,A}(t)\,\bar{i}_A(t) + v_{c,B}(t)\,\bar{i}_B(t) + v_{c,C}(t)\,\bar{i}_C(t)\right] \tag{12-19}$$

Substituting for the control voltages from Eq. 12-10 and for the output currents from Eq. 12-15 into Eq. 12-19

$$\bar{i}_d(t) = 0.5\frac{\hat{V}_c}{\hat{V}_{tri}}\hat{I}\begin{bmatrix}\sin(\omega_1 t)\sin(\omega_1 t - \phi_1) + \sin(\omega_1 t - 120^o)\sin(\omega_1 t - \phi_1 - 120^o)\\ +\sin(\omega_1 t - 240^o)\sin(\omega_1 t - \phi_1 - 240^o)\end{bmatrix} \tag{12-20}$$

that simplifies to a dc current

$$\overline{i}_d(t) = I_d = \frac{3}{4}\frac{\hat{V}_c}{\hat{V}_{tri}}\hat{I}\cos\phi_1 \tag{12-21}$$

Substituting Eq. 12-14 into Eq. 12-21

$$V_d\overline{i}_d(t) = \frac{3}{2}\hat{V}\,\hat{I}\cos\phi_1 \tag{12-22}$$

which shows that the average power input at the voltage-port equals the total three-phase power out of the current-port in this converter that is assumed loss-less.

In Fig. 12-10a, the instantaneous quantities associated with this switch-mode converter are pulsating, as shown in Fig. 12-11. Based on the discussion of harmonic components in the voltage at the current-port and the current at the voltage-port of each power-pole, we can calculate cancellation of some harmonics in the combination of the three power-poles in this ac-drive converter. A detailed discussion of this can be found in reference [1].

12-4-1 Space Vector Pulse Width Modulation

The above method of synthesizing the three-phase sinusoidal output is called the sinusoidal-PWM. As discussed in the appendix to this chapter on the accompanying CD, the sinusoidal-PWM is near ideal, except it does not utilize the available dc-link voltage to its fullest. A modified PWM technique called the space vector PWM (SV-PWM) is described in the Appendix on the accompanying CD, which can produce from the same dc-link voltage a three-phase output voltage that is higher by approximately fifteen percent.

12-5 VOLTAGE-LINK STRUCTURE WITH BI-DIRECTIONAL POWER FLOW

In many applications of ac-motor drives, the voltage-link structure in Fig. 12-1 is such that the power flow through it is bi-directional. Normally, power flows from the utility to the motor, and while slowing down, the energy stored in the inertia of machine-load combination is recovered by operating the machine as a generator and feeding power back into the utility grid. This can be accomplished by using three-phase converters discussed in section 12-4 at both ends, as shown in Fig. 12-13a, recognizing that the power flow through these converters is bi-directional. In the normal mode, converter at the utility-end operates as a rectifier and the converter at the machine-end as an inverter. The roles of these two are opposite when the power flows in the reverse direction during energy recovery.

The average representation of these converters by means of ideal transformers is shown in Fig. 12-13b. In this simplified representation, where losses are ignored, the utility source is represented by a source v_{sa}, etc. in series with the internal system inductance L_s. The machine is represented by its steady state equivalent circuit, the machine equivalent inductance L_{eq} in series with the back-emf e_A, etc. Under balanced three-phase operation at both ends, the role of each converter can be analyzed by means of the per-phase equivalent circuits shown in Fig. 12-13c. In these per-phase equivalent circuits, the fundamental-frequency voltages produced at the ac-side by the two converters are v_{a1} and v_{An1}, and the ac-side currents at the two sides can be expressed in the phasor form as

$$\bar{I}_{a1} = \frac{\bar{V}_{sa} - \bar{V}_{a1}}{j\omega_s L_s} \tag{12-23}$$

$$\bar{I}_{A1} = \frac{\bar{V}_{An1} - \bar{E}_A}{j\omega_1 L_{eq}} \tag{12-24}$$

where, the phasors in Eq. 12-23 represent voltages and current at the utility-system frequency ω_s typically 60 (or 50 Hz), and the phasors in Eq. 12-24 at the fundamental-frequency ω_1 synthesized by the machine-side converter.

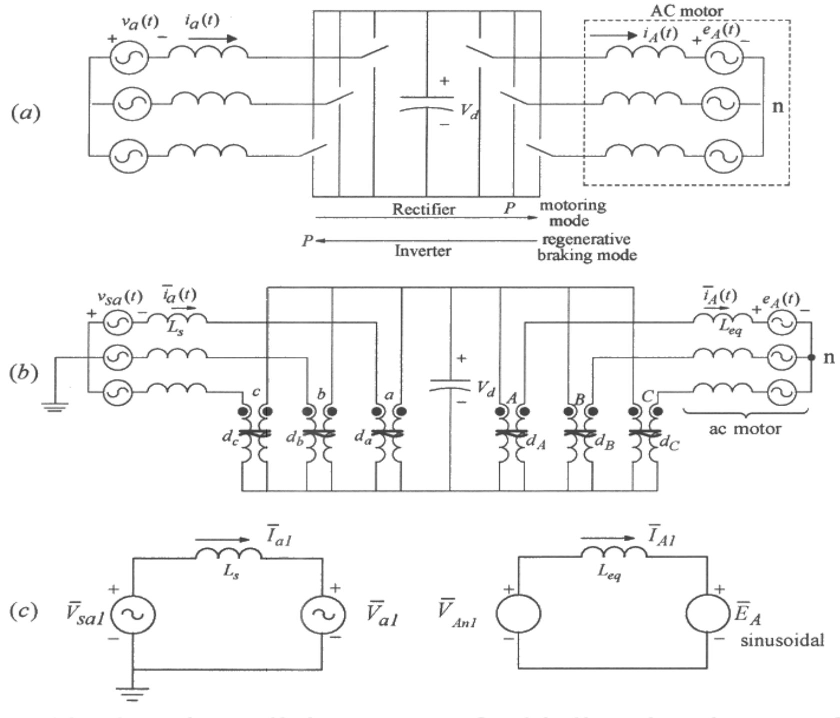

(a)
$v_a(t)$
$i_a(t)$
+
−
AC motor
$i_A(t)$
$e_A(t)$
V_d
n
Rectifier
P
motoring mode
P
Inverter
regenerative braking mode
(b)
$v_{sa}(t)$
$\bar{i}_a(t)$
L_s
c
b
a
d_c
d_b
d_a
V_d
A
B
C
d_A
d_B
d_C
$\bar{i}_A(t)$
$e_A(t)$
L_{eq}
n
ac motor
(c)
$\bar{V}_{sa1}$
$\bar{I}_{a1}$
L_s
$\bar{V}_{a1}$
$\bar{V}_{An1}$
$\bar{I}_{A1}$
L_{eq}
$\bar{E}_A$
sinusoidal

Figure 12-13 Voltage-link structure for bi-directional power flow.

In Fig. 12-13a, for a given utility voltage, it is possible to control the current drawn from the utility by controlling the voltage synthesized by the utility-side converter in magnitude and phase. In these circuits, if the losses are ignored, the average power drawn from the utility source equals the power supplied to the motor. However, the reactive power at the utility-side converter can be controlled, independently of the reactive power at the machine-side converter that depends on the motor load.

12-6 UNINTERRUPTIBLE POWER SUPPLIES (UPS)

In considering the synthesis of a low-frequency ac from a dc voltage, the uninterruptible power supplies (UPS) can be considered as a special case of ac-motor drives. UPS are used to provide power to critical loads in industry, business and medical facilities to which power should be available continuously, even during momentary utility power outages. The Computer Business Equipment Manufactures Association (CBEMA) has specifications that show the voltage tolerance envelope as a function of time. This CBEMA curve shows that the UPS for critical loads are needed, not just for complete power outages but also for "swells" and "sags" in the equipment voltage due to disturbances on the utility grid.

In a UPS, a voltage-link structure shown in Fig. 12-1 is used where the dc-link consists of batteries to shield critical loads from voltage disturbances, as shown in the block diagram of Fig. 12-14. Normally, the power to the load is provided through the two converters, where the utility-side converter also keeps the batteries charged. In the event of power-line outages, energy stored in the batteries allows load power to be supplied continuously. The function of the load-side inverter is to produce, from dc source, ac voltages similar to that in ac-motor drives, except it is a special case where the output voltage has constant specified magnitude and frequency (e.g., 115 V rms, and 60 Hz). The load may be three-phase, where the analysis of section 12-5 applies. In the following section, the case of a single-phase load is considered, since the three-phase case is similar to that in motor drives.

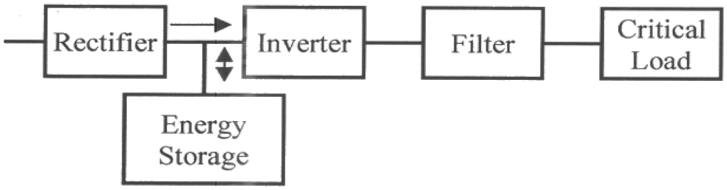


Figure 12-14 Bock diagram of UPS.

12-6-1 Single-Phase UPS

The load-side converter of 1-phase UPS is similar in power topology to that in dc-motor drives, as shown in Fig. 12-15a. The average representation is shown in Fig. 12-15b. It consists of two switching power-poles, where as shown, the inductance of the low-pass filer establishes

the current-ports of the two power-poles. The control voltage is at the desired output frequency to produce the desired output voltage amplitude:

$$v_c(t) = \hat{V}_c \sin \omega_1 t \tag{12-25}$$

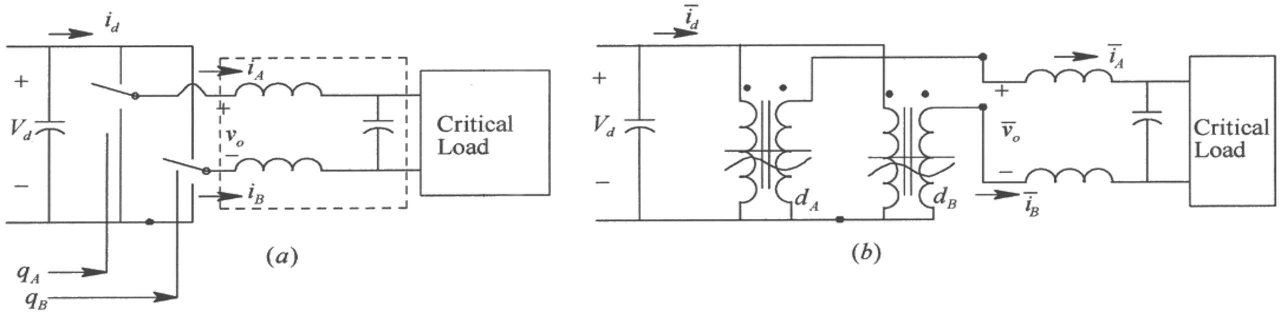


Figure 12-15 Single-phase UPS.

This control signal equals $v_{c,A}$. For the switching power-pole *B*, a phase shift of 180^0 is introduced in Eq. 12-25, that is by a factor of (-1), to produce its control signal

$$v_{c,B}(t) = \hat{V}_c \sin\left(\omega_1 t - 180^0\right) = -\hat{V}_c \sin \omega_1 t \tag{12-26}$$

As shown in Fig. 12-16a, these control signals are compared with a triangular waveform at the switching frequency, typically above 20 kHz to produce the switching functions for the transistors in the switching power-poles. The switching waveforms are shown in Fig. 12-16a.

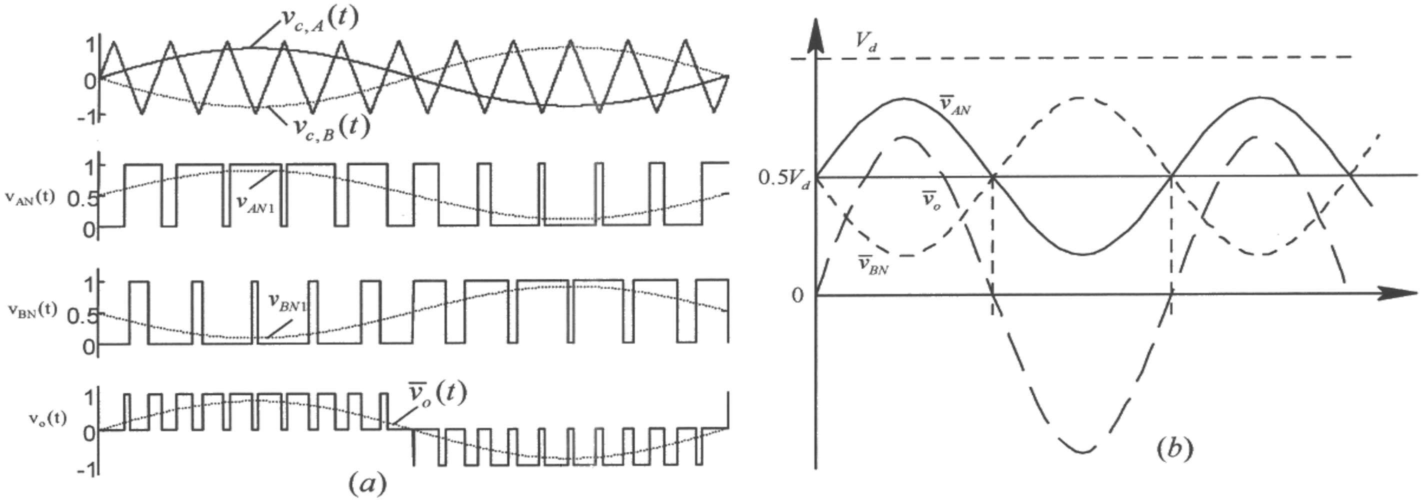


Figure 12-16 UPS waveforms.

Using the expression derived for the duty-ratio in phase *A* in Eq. 12-1, and substituting the control voltage for the other pole:

$$\begin{aligned} d_A(t) &= 0.5 + 0.5\frac{\hat{V}_c}{\hat{V}_{tri}}\sin\omega_1 t \\ d_B(t) &= 0.5 - 0.5\frac{\hat{V}_c}{\hat{V}_{tri}}\sin\omega_1 t \end{aligned} \tag{12-27}$$

With these duty-ratios, the average outputs of the two power-poles and the average output voltage $\overline{v}_o(t)$ are as follows, plotted in Fig. 12-16b

$$\begin{aligned} \overline{v}_{AN}(t) &= 0.5V_d + 0.5\frac{\hat{V}_c}{\hat{V}_{tri}}V_d\sin\omega_1 t \\ \overline{v}_{BN}(t) &= 0.5V_d - 0.5\frac{\hat{V}_c}{\hat{V}_{tri}}V_d\sin\omega_1 t \\ \overline{v}_o(t) &= \overline{v}_{AN}(t) - \overline{v}_{BN}(t) = \frac{\hat{V}_c}{\hat{V}_{tri}}V_d\sin\omega_1 t \end{aligned} \tag{12-28}$$

where,

$$\hat{V}_o = \frac{\hat{V}_c}{\hat{V}_{tri}}V_d \tag{12-29}$$

In order to calculate the average current drawn from the dc source, we will assume that the average ac-side current is sinusoidal and lagging behind the output ac voltage by an angle ϕ_1, as shown in Fig. 12-17:

$$\overline{i}_o(t) = \hat{I}_o\sin(\omega_1 t - \phi_1) \tag{12-30}$$

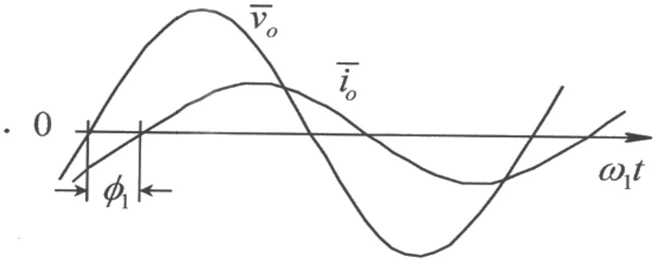


Figure 12-17 Output voltage and current.

Therefore, equating average input power to the output power, the average input current is

$$\begin{aligned} \overline{i}_d &= \frac{\overline{v}_o\overline{i}_o}{V_d} = \frac{\hat{V}_c}{\hat{V}_{tri}}\hat{I}_o\sin\omega_1 t \times \sin(\omega_1 t - \phi_1) \\ &= \underbrace{0.5\frac{\hat{V}_c}{\hat{V}_{tri}}\hat{I}_o}_{I_d} \underbrace{- 0.5\frac{\hat{V}_c}{\hat{V}_{tri}}\hat{I}_o\sin(2\omega_1 t - \phi_1)}_{i_{d2}(t)} \end{aligned} \tag{12-31}$$

which shows that the average current drawn from the dc source has a dc component I_d that is responsible for the average power transfer to the ac side of the converter, and a second harmonic component i_{d2} (at twice the frequency of the ac output), which is undesirable. The dc-link storage in a 1-phase inverter must be sized to accommodate the flow of this large ac current at twice the output frequency, similar to that in *PFC*s discussed in Chapter 6. Of course, we should not forget that the above discussion is in terms of average representation of the switching power-poles. Therefore, the dc-link storage must also accommodate the flow of switching-frequency ripple in i_d discussed below.

The switching waveforms in the single-phase UPS are shown in Fig. 12-16a, which confirm that the voltage $v_o(t)$ and $i_d(t)$ are pulsating at the switching frequency. A low-pass filter is necessary to remove the output voltage harmonic frequencies, which were discussed earlier in a generic manner for each switching power-pole. The pulsating current ripple in $i_d(t)$ can be by-passed from being supplied by the batteries by placing a small high quality capacitor with a very low equivalent series inductance.

REFERENCES

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.

PROBLEMS

Switching Power-Pole

12-1 In a switch-mode converter pole-*A*, $V_d = 150V$, $\hat{V}_{tri} = 5V$, and $f_s = 20kHz$. Calculate the values of the control signal $v_{c,A}$ and the pole duty-ratio d_A during which the switch is in its top position, for the following values of the average output voltage: $\overline{v}_{AN} = 125V$ and $\overline{v}_{AN} = 50V$.

12-2 In a converter pole, the $i_A(t)$ waveform is as shown in Fig. 12-5b. Including the ripple, show that the current relationship of an ideal transformer is valid.

DC-Motor Drives

12-3 A switch-mode dc-dc converter uses a PWM-controller IC which has a triangular waveform signal at 25 *kHz* with $\hat{V}_{tri}$ = 3 *V*. If the input dc source voltage $V_d = 150V$, calculate the gain k_{PWM} in Eq. 12-6 of this switch-mode amplifier.

12-4 In a switch-mode dc-dc converter, $v_c/\hat{V}_{tri} = 0.8$ with a switching frequency $f_s = 20\,kHz$ and $V_d = 150V$. Calculate and plot the ripple in the output voltage $v_o(t)$.

12-5 A switch-mode dc-dc converter is operating at a switching frequency of 20 *kHz*, and V_d = 150 *V*. The average current being drawn by the dc motor is 8.0 A. In the equivalent circuit of the dc motor, $E_a = 100V$, $R_a = 0.25\Omega$, and $L_a = 4\,mH$. (a) Plot the output current and calculate the peak-to-peak ripple, and (b) plot the dc-side current.

12-6 In Problem 12-5, the motor goes into regenerative braking mode. The average current being supplied by the motor to the converter during braking is 8.0 *A*. Plot the voltage and current waveforms on both sides of this converter at that this instant. Calculate the average power flow into the converter.

12-7 In Problem 12-5, calculate $\overline{i}_{dA}$, $\overline{i}_{dB}$, and $\overline{i}_d (= I_d)$.

12-8 Repeat Problem 12-5 if the motor is rotating in the reverse direction, with the same current draw and the same induced emf E_a value of the opposite polarity.

12-9 Repeat Problem 12-8 if the motor is braking while it has been rotating in the reverse direction. It supplies the same current and produces the same induced emf E_a value of the opposite polarity.

12-10 Repeat problem 12-5 if a bi-polar voltage switching is used in the dc-dc converter. In such a switching scheme, the two bi-positional switches are operated in such a manner that when switch-*A* is in the top position, switch-*B* is in its bottom position, and vice versa. The switching signal for pole-*A* is derived by comparing the control voltage (as in Problem 12-5) with the triangular waveform.

Three-Phase AC-Motor Drives

12-11 Plot $d_A(t)$ if the output voltage of the converter pole-*A* is $\overline{v}_{AN}(t) = \frac{V_d}{2} + 0.85\frac{V_d}{2}\sin(\omega_1 t)$, where $\omega_1 = 2\pi \times 60\,rad/s$.

12-12 In a three-phase dc-ac inverter, $V_d = 300V$, $\hat{V}_{tri} = 1V$, $\hat{V}_c = 0.75V$, and $f_1 = 45\,Hz$. Calculate and plot $d_A(t), d_B(t), d_C(t)$, $\overline{v}_{AN}(t), \overline{v}_{BN}(t), v_{CN}(t)$, and $\overline{v}_{An}(t)$, $\overline{v}_{Bn}(t)$, and $\overline{v}_{Cn}(t)$.

12-13 In a balanced three-phase dc-ac inverter, the phase-*A* average output voltage is $\overline{v}_{An}(t) = \frac{V_d}{2} 0.75\sin(\omega_1 t)$, where $V_d = 300V$ and $\omega_1 = 2\pi \times 45\,rad/s$. The inductance L in each phase is 5 *mH*. The ac-motor internal voltage in phase *A* can be represented as $e_A(t) = 106.14\sin(\omega_1 t - 6.6^0)V$. (a) Calculate and plot $d_A(t)$, $d_B(t)$, and $d_C(t)$, and (b) sketch $\overline{i}_A(t)$ and $\overline{i}_{dA}(t)$.

12-14 In Problem 12-13, calculate and plot $\overline{i}_d(t)$, which is the average dc current drawn from the dc-side.

Single-Phase UPS

12-15 In a 1-phase UPS, $V_d = 300V$, $\overline{v}_o(t) = 170\sin(2\pi \times 60t)\ V$, and $\overline{i}_o(t) = 10\sin(2\pi \times 60t - 30^o)\ A$. Calculate and plot $d_A(t)$, $d_B(t)$, $\overline{v}_{AN}(t)$, $\overline{v}_{BN}(t)$, I_d, $i_{d2}(t)$, and $\overline{i}_d(t)$.

12-16 In Problem 12-15, calculate $q_A(t)$ and $q_B(t)$ at $\omega t = 90^0$.

Chapter 13

DESIGNING FEEDBACK CONTROLLERS FOR MOTOR DRIVES

13-1 INTRODUCTION

Many applications, such as robotics and factory automation, require precise control of speed and position. In such applications, a feedback control, as illustrated by Fig. 13-1, is used. This feedback control system consists of a power-processing unit (PPU), a motor, and a mechanical load. The output variables such as torque and speed are sensed and are fed back, to be compared with the desired (reference) values. The error between the reference and the actual values are amplified to control the power-processing unit to minimize or eliminate this error. A properly designed feedback controller makes the system insensitive to disturbances and changes in the system parameters.

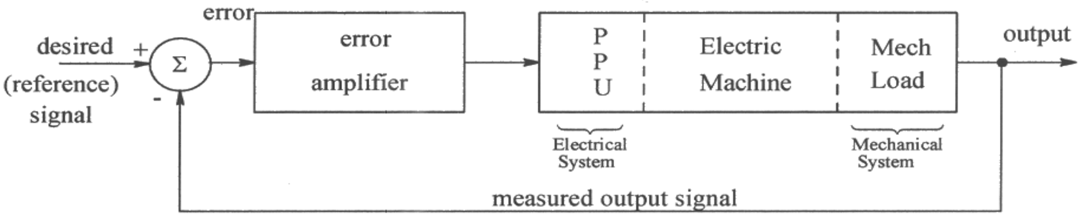


Fig 13-1 Feedback controlled drive.

The objective of this chapter is to discuss the design of motor-drive controllers. A dc-motor drive is used as an example, although the same design concepts can be applied in controlling brushless-dc motor drives and vector-controlled induction-motor drives. In the following discussion, it is assumed that the power-processing unit is of a switch-mode type and has a very fast response time. A permanent-magnet dc machine with a constant field flux ϕ_f is assumed.

13-2 CONTROL OBJECTIVES

The control system in Fig. 13-1 is shown simplified in Fig. 13-2, where $G_p(s)$ is the Laplace-domain transfer function of the plant consisting of the power-processing unit, the motor, and the mechanical load. $G_c(s)$ is the controller transfer function. In response to a desired (reference) input $X^*(s)$, the output of the system is $X(s)$, which (ideally) equals the reference input. The controller $G_c(s)$ is designed with the following objectives in mind:

- a zero steady state error.
- a good dynamic response (which implies both a fast transient response, for example to a step-change in the input, and a small settling time with very little overshoot).

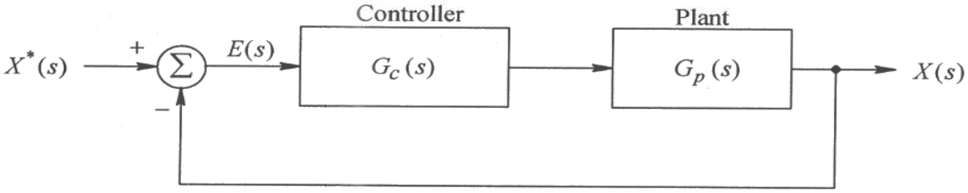


Fig 13-2 Simplified control system representation.

To keep the discussion simple, a unity feedback will be assumed. The open-loop transfer function (including the forward path and the unity feedback path) $G_{OL}(s)$ is

$$G_{OL}(s) = G_c(s)G_p(s) \tag{13-1}$$

The closed-loop transfer function $\dfrac{X(s)}{X^*(s)}$ in a unity feedback system is

$$G_{CL}(s) = \frac{G_{OL}(s)}{1+G_{OL}(s)} \tag{13-2}$$

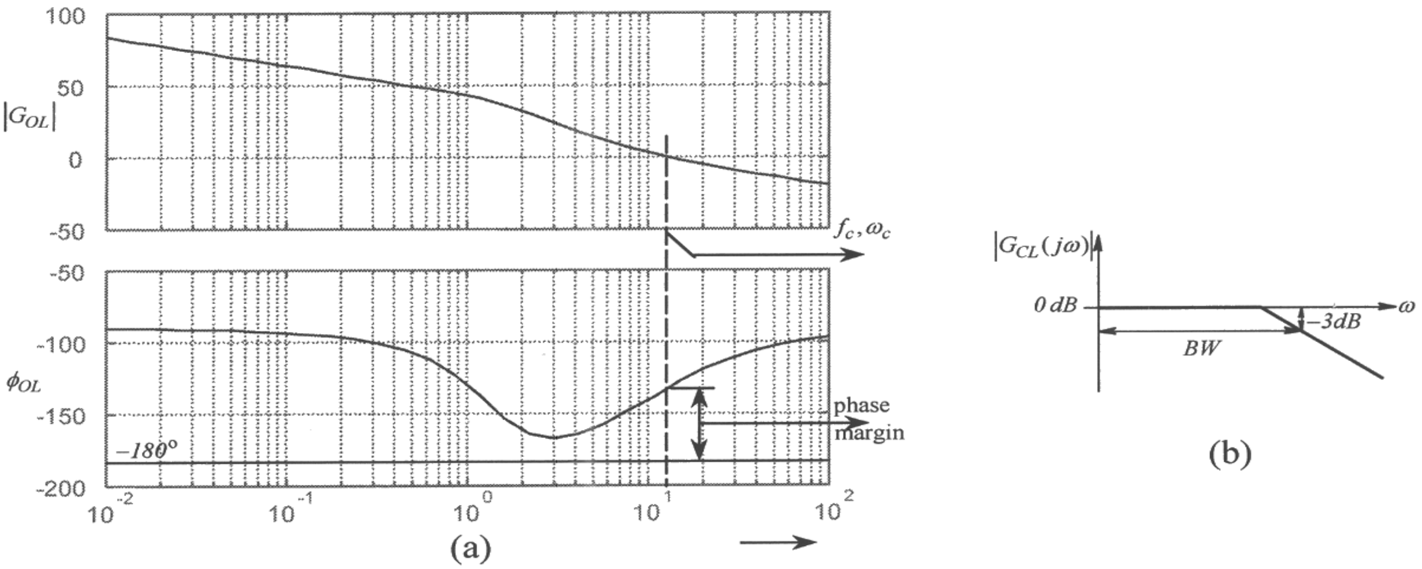
In order to define a few necessary control terms, we will consider a generic Bode plot of the open-loop transfer function $G_{OL}(s)$ in terms of its magnitude and phase angle, shown in Fig. 13-3a as a function of frequency. The frequency at which the gain equals unity (that is $|G_{OL}(s)| = 0db$) is defined as the crossover frequency f_c (angular frequency ω_c). At the crossover frequency, the phase delay introduced by the open-loop transfer function must be less than 180^0 in order for the closed-loop feedback system to be stable. Therefore, at f_c, the phase angle $\phi_{OL}|_{f_c}$ of the open-loop transfer function, measured with respect to -180^0, is defined as the Phase Margin (PM):

$$\text{Phase Margin (PM)} = \phi_{OL}|_{f_c} - (-180^0) = \phi_{OL}|_{f_c} + 180^0 \tag{13-3}$$

Note that $\phi_{OL}|_{f_c}$ has a negative value. For a satisfactory dynamic response without oscillations, the phase margin should be greater than 45^0, preferably close to 60^0.

The magnitude of the closed-loop transfer function is plotted in Fig. 13-3b (idealized by the asymptotes), in which the bandwidth is defined as the frequency at which the gain drops to (–3 dB). As a first-order approximation in many practical systems,

$$\text{Closed-loop bandwidth} \approx f_c \tag{13-4}$$



(a)

(b)

Figure 13-3 (a) Phase Margin; (b) bandwidth.

For a fast transient response by the control system, for example a response to a step-change in the input, the bandwidth of the closed-loop should be high. From Eq. 13-4, this requirement implies that the crossover frequency f_c (of the open-loop transfer function shown in Fig. 13-3a) should be designed to be high.

13-3 CASCADE CONTROL STRUCTURE

In the following discussion, a cascade control structure such as that shown in Fig. 13-4 is used. The cascade control structure is commonly used for motor drives because of its flexibility. It consists of distinct control loops; the innermost current (torque) loop is followed by the speed loop. If position needs to be controlled accurately, the outermost position loop is superimposed on the speed loop. Cascade control requires that the bandwidth (speed of response) increase towards the inner loop, with the torque loop being the fastest and the position loop being the slowest. The cascade control structure is widely used in industry.

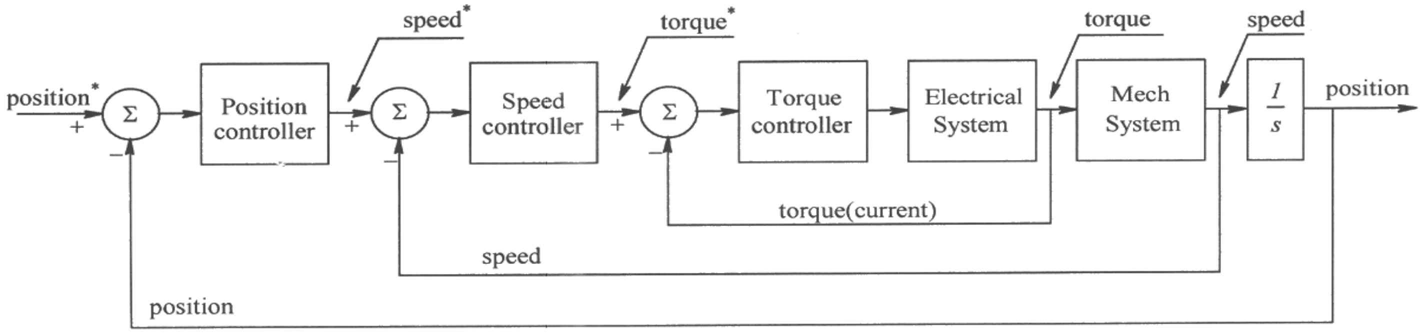

position*
+
−
Σ
Position controller
speed*
+
−
Σ
Speed controller
torque*
+
−
Σ
Torque controller
Electrical System
torque
Mech System
speed
$\frac{1}{s}$
position
torque(current)
speed
position

Figure 13-4 Cascade control of a motor drive.

13-4 STEPS IN DESIGNING THE FEEDBACK CONTROLLER

Motion control systems often must respond to large changes in the desired (reference) values of the torque, speed, and position. They must reject large, unexpected load disturbances. For large changes, the overall system is often nonlinear. This nonlinearity comes about because the mechanical load is often highly nonlinear. Additional nonlinearity is introduced by voltage and current limits imposed by the power-processing unit and the motor. In view of the above, the following steps for designing the controller are suggested:

1. The first step is to assume that, around the steady-state operating point, the input reference changes and the load disturbances are all small. In such a small-signal analysis, the overall system can be assumed to be linear around the steady-state operating point, thus allowing the basic concepts of linear control theory to be applied.
2. Based on the linear control theory, once the controller has been designed, the entire system can be simulated on a computer under large-signal conditions to evaluate the adequacy of the controller. The controller must be "adjusted" as appropriate.

13-5 SYSTEM REPRESENTATION FOR SMALL-SIGNAL ANALYSIS

For ease of the analysis described below, the system in Fig. 13-4 is assumed linear and the steady-state operating point is assumed to be zero for all of the system variables. This linear analysis can be then extended to nonlinear systems and to steady-state operating conditions other than zero. The control system in Fig. 13-4 is designed with the highest bandwidth (associated with the torque loop), which is one or two orders of magnitude smaller than the switching frequency f_s. As a result, in designing the controller, the switching-frequency components in various quantities are of no consequence. Therefore, we will use the average variables discussed in Chapter 3, where the switching-frequency components were eliminated.

13-5-1 The Average Representation of the Power-Processing Unit (PPU)

For the purposes of designing the feedback controller, we will assume that the dc-bus voltage V_{dc} within the PPU shown in Fig. 13-5a is constant. Following the averaging analysis in Chapter 3, the average representation of the switch-mode converter is shown in Fig. 13-5b. In terms of the dc-bus voltage V_{dc} and the triangular-frequency waveform peak $\hat{V}_{tri}$, the average output voltage $\overline{v}_a(t)$ of the converter is linearly proportional to the control voltage:

$$\overline{v}_a(t) = k_{PWM}\, v_c(t) \qquad \left(k_{PWM} = \frac{V_{dc}}{\hat{V}_{tri}}\right) \tag{13-5}$$

where k_{PWM} is the gain constant of the PWM converter. Therefore, in Laplace domain, the PWM controller and the dc-dc switch-mode converter can be represented simply by a gain-constant k_{PWM}, as shown in Fig. 13-5c:

$$V_a(s) = k_{PWM} V_c(s) \tag{13-6}$$

where $V_a(s)$ is the Laplace transform of $\overline{v}_a(t)$, and $V_c(s)$ is the Laplace transform of $v_c(t)$. The above representation is valid in the linear range, where $-\hat{V}_{tri} \le v_c \le \hat{V}_{tri}$.

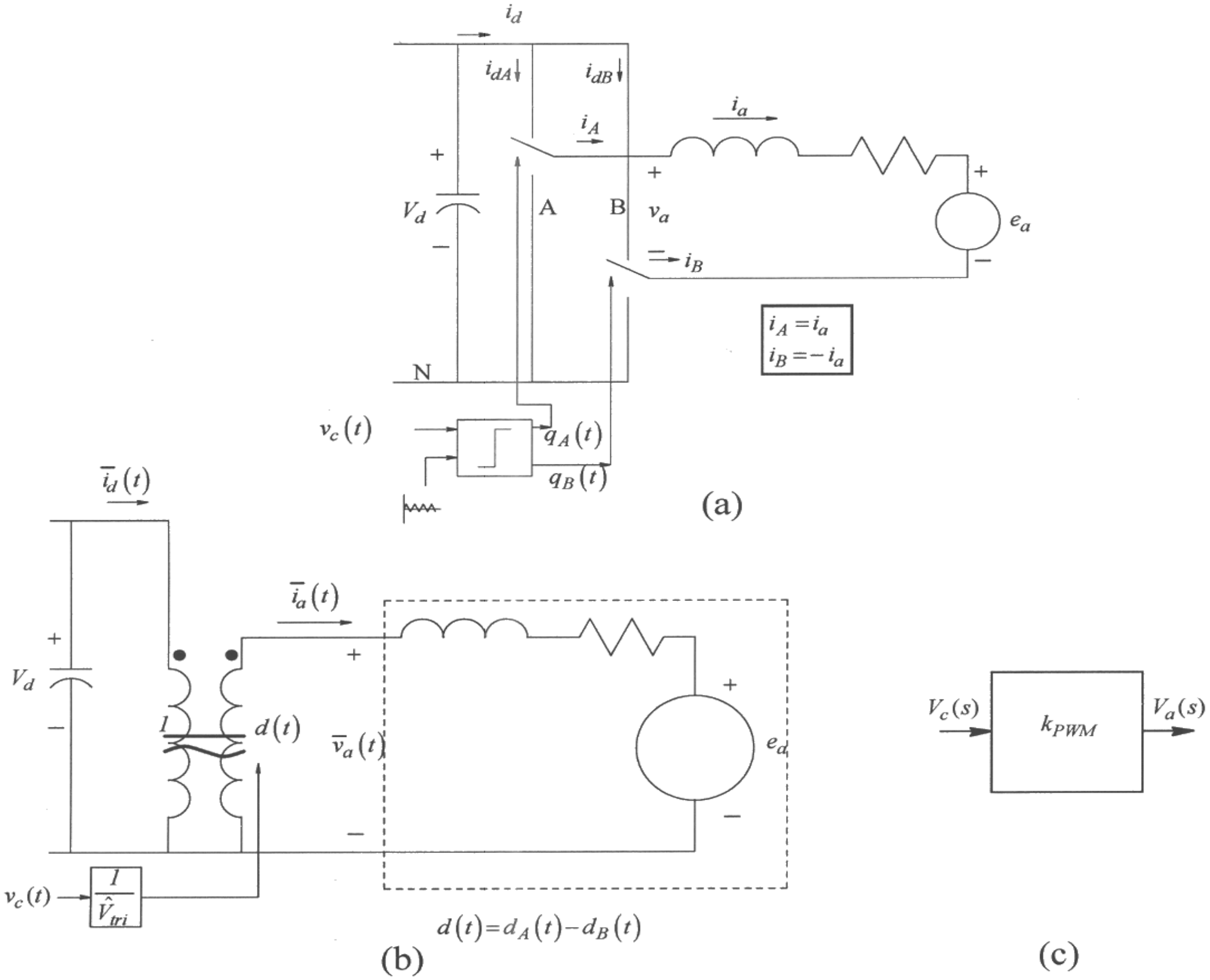

i_d
i_{dA}
i_{dB}
i_A
i_a
+
V_d
−
A
B
+
v_a
−
i_B
+
e_a
−
$i_A = i_a$
$i_B = -i_a$
N
$v_c(t)$
$q_A(t)$
$q_B(t)$
(a)
$\overline{i}_d(t)$
$\overline{i}_a(t)$
+
V_d
−
1
$d(t)$
+
$\overline{v}_a(t)$
−
+
e_a
−
$v_c(t)$
$\frac{1}{\hat{V}_{tri}}$
$d(t) = d_A(t) - d_B(t)$
(b)
$V_c(s)$
k_{PWM}
$V_a(s)$
(c)

Figure 13-5 (a) Switch-mode converter for dc motor drives; (b) average model of the switch-mode converter; (c) linearized representation.

13-5-2 Modeling of the DC Machine and the Mechanical Load

The dc motor and the mechanical load are modeled as shown by the equivalent circuit in Fig. 13-6a, in which the speed $\omega_m(t)$ and the back-emf $e_a(t)$ are assumed not to contain switching-frequency components. The electrical and the mechanical equations corresponding to Fig. 13-6a are

$$\overline{v}_a(t) = e_a(t) + R_a \overline{i}_a(t) + L_a \frac{d}{dt}\overline{i}_a(t), \qquad e_a(t) = k_E \omega_m(t) \tag{13-7}$$

and

$$\frac{d}{dt}\omega_m(t) = \frac{\overline{T}_{em}(t) - T_L}{J_{eq}}, \qquad \overline{T}_{em}(t) = k_T \overline{i}_a(t) \tag{13-8}$$

where the equivalent load inertia $J_{eq} (= J_M + J_L)$ is the sum of the motor inertia and the load inertia, and the damping is neglected (it could be combined with the load torque T_L). In the simplified procedure presented here, the controller is designed to follow the changes in the torque, speed, and position reference values (and hence the load torque in Eq. 13-8 is assumed to be absent). Eqs. 13-7 and 13-8 can be expressed in the Laplace domain as

$$V_a(s) = E_a(s) + (R_a + sL_a) I_a(s) \tag{13-9}$$

or

$$I_a(s) = \frac{V_a(s) - E_a(s)}{R_a + sL_a}, \qquad E_a(s) = k_E\, \omega_m(s) \tag{13-10}$$

We can define the Electrical Time Constant τ_e as

$$\tau_e = \frac{L_a}{R_a} \tag{13-11}$$

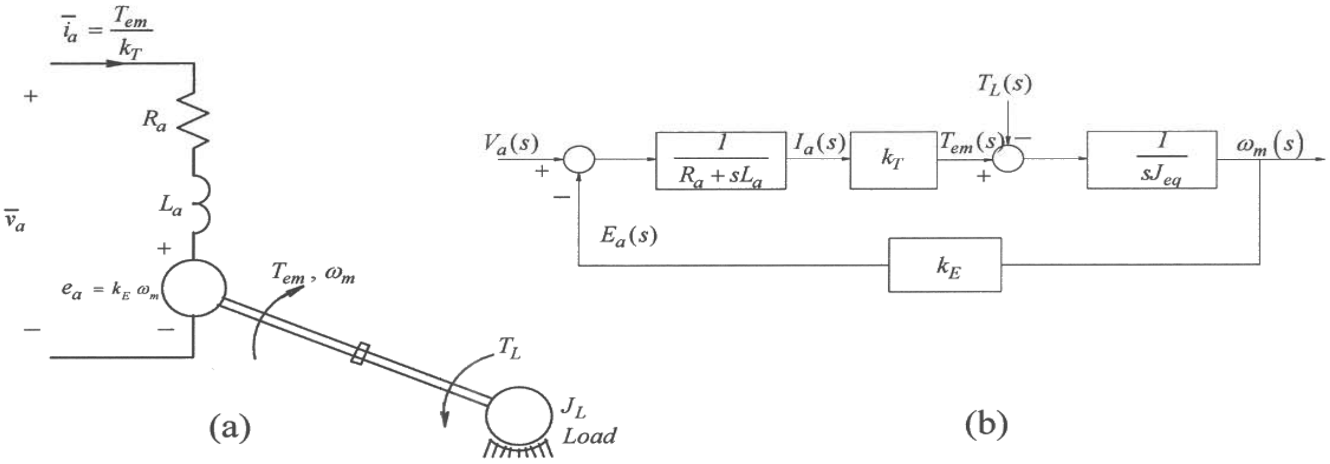
Therefore, Eq. 13-10 can be written in terms of τ_e as

$$I_a(s) = \frac{1/R_a}{1 + \dfrac{s}{1/\tau_e}} \{V_a(s) - E_a(s)\}, E_a(s) = k_E\, \omega_m(s) \tag{13-12}$$

From Eq. 13-8, assuming the load torque to be absent in the design procedure,

$$\omega_m(s) = \frac{T_{em}(s)}{sJ_{eq}}, T_{em}(s) = k_T I_a(s) \tag{13-13}$$

Eqs. 13-10 and 13-13 can be combined and represented in block-diagram form, as shown in Fig. 13-6b.



(a) (b)

Fig 13-6 DC motor and mechanical load (a) equivalent circuit; (b) block diagram.

13-6 CONTROLLER DESIGN

The controller in the cascade control structure shown in Fig. 13-4 is designed with the objectives discussed in section 13-2 in mind. In the following section, a simplified design procedure is described.

13-6-1 PI Controllers

Motion control systems often utilize a proportional-integral (PI) controller, as shown in Fig. 13-7. The input to the controller is the error $E(s) = X^*(s) - X(s)$, which is the difference between the reference input and the measured output.

In Fig. 13-7, the proportional controller produces an output proportional to the error input:

$$V_{c,p}(s) = k_p E(s) \tag{13-14}$$

where k_p is the proportional-controller gain. In torque and speed loops, proportional controllers, if used alone, result in a steady-state error in response to step-change in the input reference. Therefore, they are used in combination with the integral controller described below.

In the integral controller shown in Fig. 13-7, the output is proportional to the integral of the error $E(s)$, expressed in the Laplace domain as

$$V_{c,i}(s) = \frac{k_i}{s} E(s) \tag{13-15}$$

where k_i is the integral-controller gain. Such a controller responds slowly because its action is proportional to the time integral of the error. The steady-state error goes to zero for a step-change in input because the integrator action continues for as long as the error is not zero.

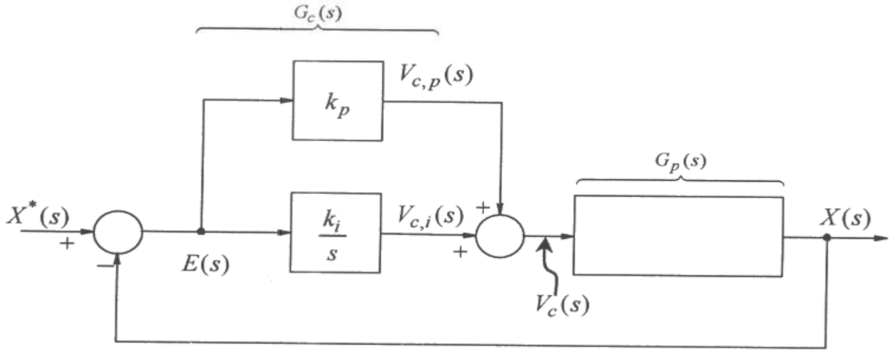


Figure 13-7 PI controller.

In motion-control systems, the P controllers in the position loop and the PI controllers in the speed and torque loop are often adequate. Therefore, we will not consider differential (D) controllers. As shown in Fig. 13-7, $V_c(s) = V_{c,p}(s) + V_{c,i}(s)$. Therefore, using Eqs. 13-14 and 13-15, the transfer function of a PI controller is

$$\frac{V_c(s)}{E(s)} = (k_p + \frac{k_i}{s}) = \frac{k_i}{s}[1 + \frac{s}{k_i / k_p}] \qquad (13\text{-}16)$$

13-7 EXAMPLE OF A CONTROLLER DESIGN

In the following discussion, we will consider the example of a permanent-magnet dc-motor supplied by a switch-mode PWM dc-dc converter. The system parameters are given as follows in Table 13-1:

Table 13-1 DC-Motor Drive System

System Parameter	Value
R_a	2.0Ω
L_a	$5.2 mH$
J_{eq}	$152 \times 10^{-6} kg \cdot m^2$
B	0
K_E	$0.1 V/(rad/s)$
k_T	$0.1 Nm/A$
V_d	$60 V$
$\hat{V}_{tri}$	$5 V$
f_s	$33 kHz$

We will design the torque, speed, and position feedback controllers (assuming a unity feedback) based on the small-signal analysis, in which the load nonlinearity and the effects of the limiters can be ignored.

13-7-1 The Design of the Torque (Current) Control Loop

As mentioned earlier, we will begin with the innermost loop in Fig. 13-8a (utilizing the transfer function block diagram of Fig. 13-6b to represent the motor-load combination, Fig. 13-5c to represent the PPU, and Fig. 13-7 to represent the PI controller).

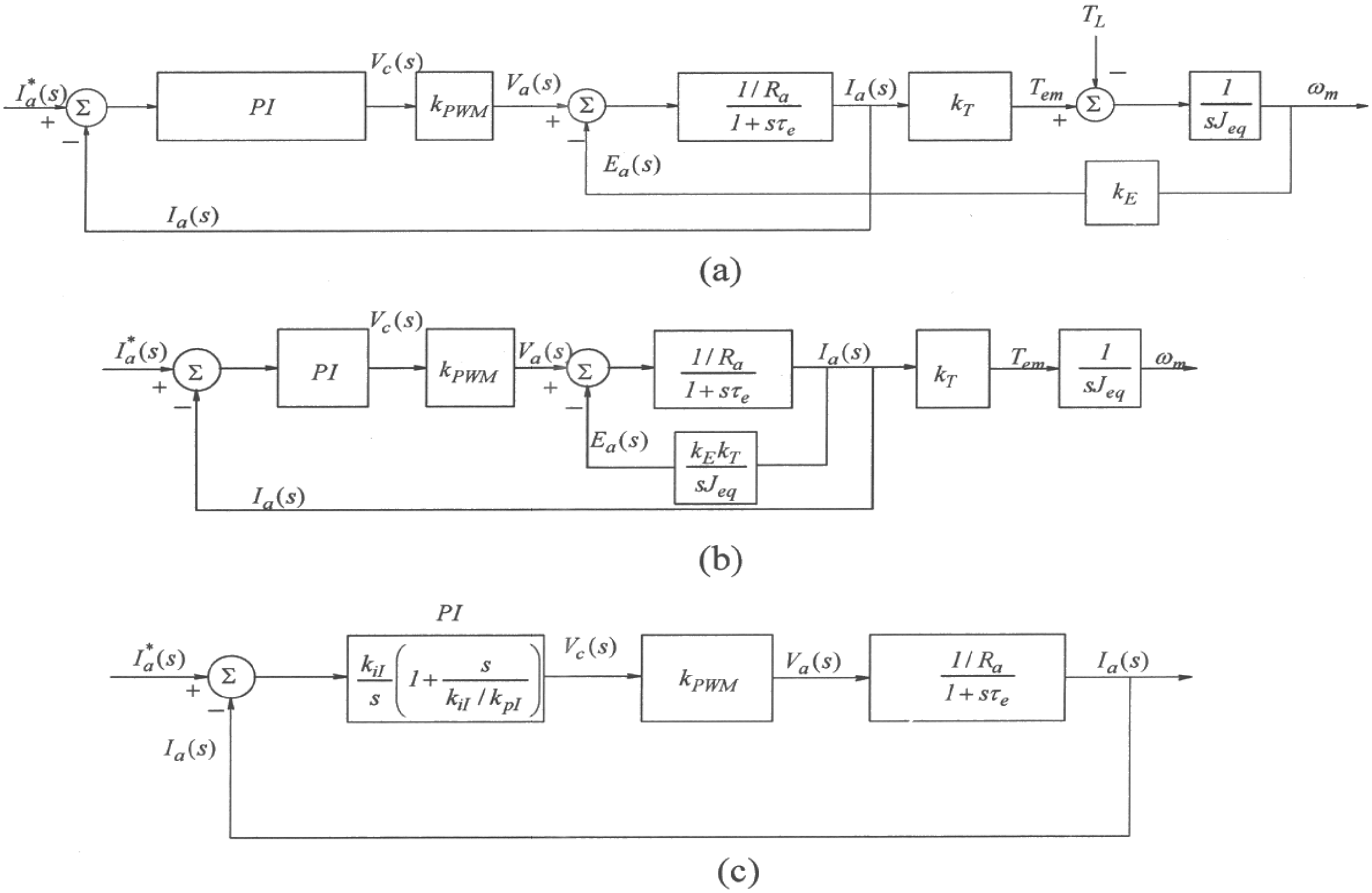

(a)
(b)
(c)
$I_a^*(s)$
Σ
+
−
PI
$V_c(s)$
k_{PWM}
$V_a(s)$
$E_a(s)$
$\frac{1/R_a}{1+s\tau_e}$
$I_a(s)$
k_T
T_L
T_{em}
$\frac{1}{sJ_{eq}}$
ω_m
k_E
$\frac{k_E k_T}{sJ_{eq}}$
$\frac{k_{iI}}{s}\left(1+\frac{s}{k_{iI}/k_{pI}}\right)$

Fig. 13-8 Design of the torque control loop.

In permanent-magnet dc motors in which ϕ_f is constant, the current and the torque are proportional to each other, related by the torque constant k_T. Therefore, we will consider the current to be the control variable because it is more convenient to use. Notice that there is a feedback in the current loop from the output speed. This feedback dictates the induced back-emf. Neglecting T_L, and considering the current to be the output, $E_a(s)$ can be calculated in terms of $I_a(s)$ in Fig. 13-8a as $E_a(s) = \frac{k_T k_E}{sJ_{eq}} I_a(s)$. Therefore, Fig. 13-8a can be redrawn as shown in Fig. 13-8b. Notice that the feedback term depends inversely on the inertia J_{eq}. Assuming that the inertia is sufficiently large to justify neglecting the feedback effect, we can simplify the block diagram, as shown in Fig. 13-8c.

The current-controller in Fig. 13-8c is a proportional-integral (PI) error amplifier with the proportional gain k_{pI} and the integral gain k_{iI}. Its transfer function is given by Eq. 13-16. The subscript "I" refers to the current loop. The open-loop transfer function $G_{I,OL}(s)$ of the simplified current loop in Fig. 13-8c is

$$G_{I,OL}(s) = \underbrace{\frac{k_{iI}}{s}[1+\frac{s}{k_{iI}/k_{pI}}]}_{PI-controller} \underbrace{k_{PWM}}_{PPU} \underbrace{\frac{1/R_a}{1+\frac{s}{1/\tau_e}}}_{motor} \qquad (13\text{-}17)$$

To select the gain constants of the PI controller in the current loop, a simple design procedure, which results in a phase margin of 90 degrees, is suggested as follows:

- Select the zero (k_{iI}/k_{pI}) of the PI controller to cancel the motor pole at $(1/\tau_e)$ due to the electrical time-constant τ_e of the motor. Under these conditions,

$$\frac{k_{iI}}{k_{pI}} = \frac{1}{\tau_e} \qquad \text{or} \qquad k_{pI} = \tau_e k_{iI} \qquad (13\text{-}18)$$

Cancellation of the pole in the motor transfer function renders the open-loop transfer function to be

$$G_{I,OL}(s) = \frac{k_{I,OL}}{s} \qquad (13\text{-}19a)$$

where

$$k_{I,OL} = \frac{k_{iI}k_{PWM}}{R_a} \qquad (13\text{-}19b)$$

- In the open-loop transfer function of Eq. 13-19a, the crossover frequency $\omega_{cI} = k_{I,OL}$. We will select the crossover frequency $f_{cI}(=\omega_{cI}/2\pi)$ of the current open-loop to be approximately one to two orders of magnitude smaller than the switching frequency of the power-processing unit in order to avoid interference in the control loop from the switching-frequency noise. Therefore, at the selected crossover frequency, from Eq. 13-19b,

$$k_{iI} = \frac{\omega_{cI}R_a}{k_{PWM}} \qquad (13\text{-}20)$$

This completes the design of the torque (current) loop, as illustrated by the example below, where the gain constants k_{pI} and k_{iI} can be calculated from Eqs. 13-18 and 13-20.

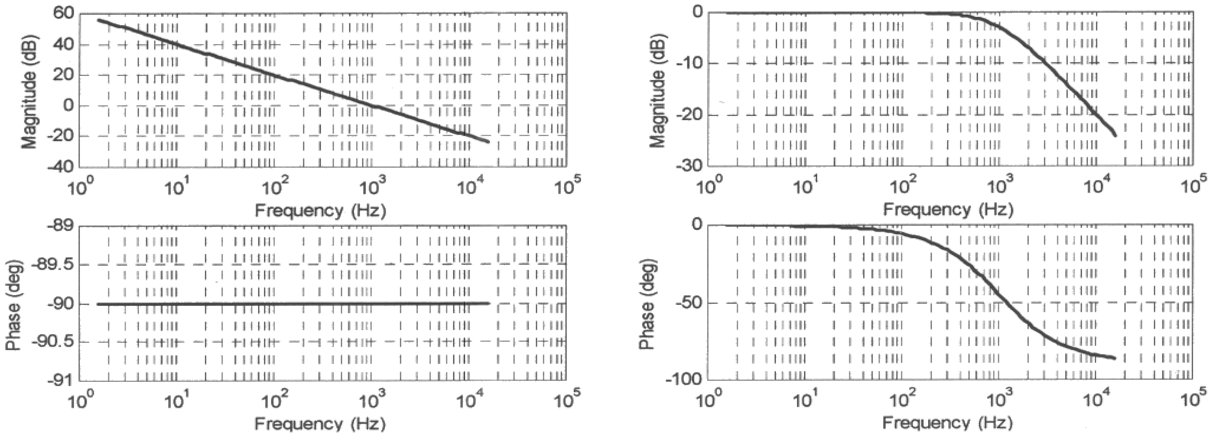
▲ **Example 13-1** Design the current loop for the example system of Table 13-1, assuming that the crossover frequency is selected to be 1 *kHz*.

Solution From Eq. 13-20, for $\omega_{cI} = 2\pi \times 10^3 rad/s$,

$$k_{iI} = \frac{\omega_{cI} R_a}{k_{PWM}} = 1050.0$$

and, from Eq. 13-18,

$$k_{pI} = k_{iI}\tau_e = k_{iI}\frac{L_a}{R_a} = 2.73\,.$$



(a) (b)

Figure 13-9 Frequency response of the current loop (a) open loop; (b) closed loop.

The open-loop transfer function is plotted in Fig. 13-9a, which shows that the crossover frequency is 1 *kHz*, as assumed previously. The closed-loop transfer function is plotted in Fig. 13-9b. ▲

13-7-2 The Design of the Speed Loop

We will select the bandwidth of the speed loop to be one order of magnitude smaller than that of the current (torque) loop. Therefore, the closed-current loop can be assumed ideal for design purposes and represented by unity, as shown in Fig. 13-10. The speed controller is of the proportional-integral (PI) type. The resulting open-loop transfer function $G_{\Omega,OL}(s)$ of the speed loop in the block diagram of Fig. 13-10 is as follows, where the subscript "Ω" refers to the speed loop:

$$G_{\Omega,OL}(s) = \underbrace{\frac{k_{i\Omega}}{s}[1+s/(k_{i\Omega}/k_{p\Omega})]}_{PI\ controller} \quad \underbrace{1}_{current\ loop} \quad \underbrace{\frac{k_T}{sJ_{eq}}}_{torque+inertia} \tag{13-21}$$

Eq. 13-21 can be rearranged as

$$G_{\Omega,OL}(s) = (\frac{k_{i\Omega}k_T}{J_{eq}})\frac{1+s/(k_{i\Omega}/k_{p\Omega})}{s^2} \tag{13-22}$$

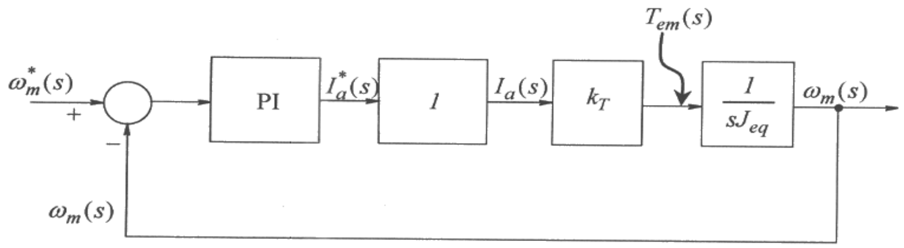


Fig 13-10 Block diagram of the speed loop.

This shows that the open-loop transfer function consists of a double pole at the origin. At low frequencies in the Bode plot, this double pole at the origin causes the magnitude to decline at the rate of – 40 db per decade while the phase angle is at -180^0. We can select the crossover frequency $\omega_{c\Omega}$ to be one order of magnitude smaller than that of the current loop. Similarly, we can choose a reasonable value of the phase margin $\phi_{pm,\Omega}$. Therefore, Eq. 13-22 yields two equations at the crossover frequency:

$$\left|(\frac{k_{i\Omega}k_T}{J_{eq}})\frac{1+s/(k_{i\Omega}/k_{p\Omega})}{s^2}\right|_{s=j\omega_{c\Omega}} = 1 \tag{13-23}$$

and

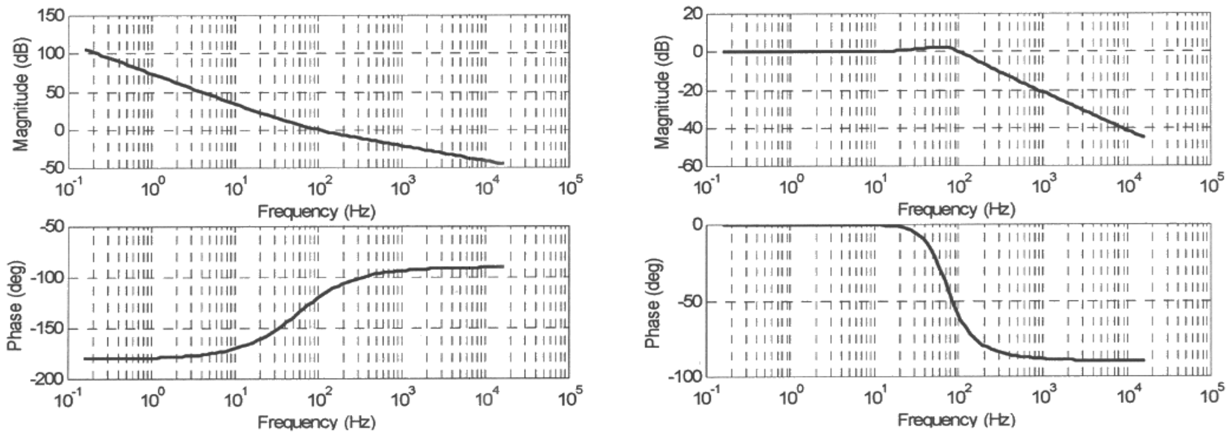
$$\angle(\frac{k_{i\Omega}k_T}{J_{eq}})\frac{1+s/(k_{i\Omega}/k_{p\Omega})}{s^2}\Bigg|_{s=j\omega_{c\Omega}} = -180^0 + \phi_{pm,\Omega} \tag{13-24}$$

The two gain constants of the PI controller can be calculated by solving these two equations, as illustrated by the following example.

▲ **Example 13-2** Design the speed loop controller, assuming the speed loop crossover frequency to be one order of magnitude smaller than that of the current loop in Example 13-2; that is, $f_{c\Omega} = 100\,Hz$, and thus $\omega_{c\Omega} = 628\,rad/s$. The phase margin is selected to be 60^0.

Solution In Eqs. 13-23 and 13-24, substituting $k_T = 0.1\,Nm/A$, $J_{eq} = 152\times10^{-6}\,kg\cdot m^2$, and $\phi_{PM,\Omega} = 60^o$ at the crossover frequency, where $s = j\omega_{c\Omega} = j628$, we can calculate that

$k_{p\Omega} = 0.827$ and $k_{i\Omega} = 299.7$.



(a) (b)

Figure 13-11 Speed loop response (a) open loop; (b) closed loop.

The open- and the closed-loop transfer functions are plotted in Figs. 13-11a and 13-11b. ▲

13-7-3 The Design of the Position Control Loop

We will select the bandwidth of the position loop to be one order of magnitude smaller than that of the speed loop. Therefore, the speed loop can be idealized and represented by unity, as shown in Fig. 13-12. For the position controller, it is adequate to have only a proportional gain $k_{p\theta}$ because of the presence of a true integrator $(1/s)$ in Fig. 13-12 in the open-loop transfer function. This integrator will reduce the steady state error to zero for a step-change in the reference position. With this choice of the controller, and with the closed–loop response of the speed loop assumed to be ideal, the open-loop transfer function $G_{\theta,OL}(s)$ is

$$G_{\theta,OL}(s) = \frac{k_\theta}{s} \tag{13-25}$$

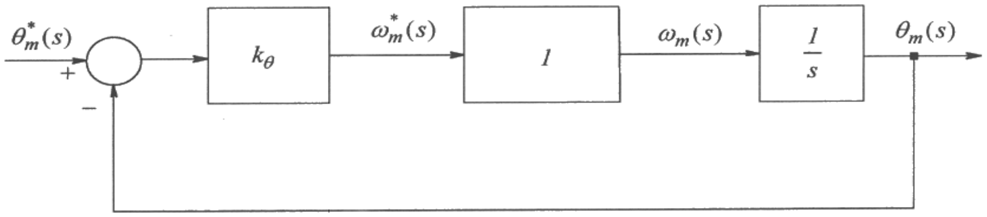


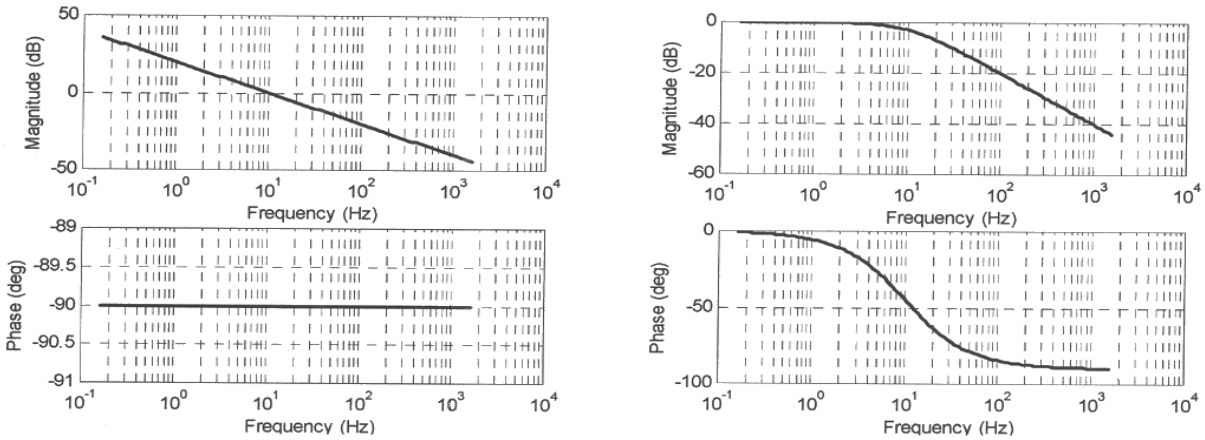
Fig 13-12 Block diagram of position loop.

Therefore, selecting the crossover frequency $\omega_{c\theta}$ of the open-loop allows k_θ to be calculated as

$$k_\theta = \omega_{c\theta} \tag{13-26}$$

▲ **Example 13-3** For the example system of Table 13-1, design the position-loop controller, assuming the position-loop crossover frequency to be one order of magnitude smaller than that of the speed loop in Example 13-3 (that is, $f_{c\theta} = 10\,Hz$ and $\omega_{c\theta} = 62.8\,rad/s$).

Solution From Eq. 13-26, $k_\theta = \omega_{c\theta} = 62.8\,rad/s$.



(a) (b

Figure 13-13 Position loop response (a) open loop; (b) closed loop.

The open- and the closed-loop transfer functions are plotted in Figs. 13-13a and 13-13b. ▲

REFERENCE

1. M. Kazmierkowski and H. Tunia, "Automatic Control of Converter-Fed Drives," Elsevier, 1994, 559 pages.

PROBLEMS

13-1 In a unity feedback system, the open-loop transfer function is of the form $G_{OL}(s) = \dfrac{k}{1 + s/\omega_p}$. Calculate the bandwidth of the closed-loop transfer function. How does the bandwidth depend on k and ω_p?

13-2 In a feedback system, the forward path has a transfer function of the form $G(s) = \dfrac{k}{1 + s/\omega_p}$, and the feedback path has a gain of k_{fb} which is less than unity. Calculate the bandwidth of the closed-loop transfer function. How does the bandwidth depend on k_{fb}?

13-3 In designing the torque loop of Example 13-1, include the effect of the back-emf, shown in Fig. 13-8a. Design a PI controller for the same open-loop crossover frequency and for a phase margin of 60 degrees. Compare your results with those in Example 13-1.

13-4 In designing the speed loop of Example 13-2, include the torque loop by a first-order transfer function based on the design in Example 13-1. Design a PI controller for the same open-loop crossover frequency and the same phase margin as in Example 13-2 and compare results.

13-5 In designing the position loop of Example 13-3, include the speed loop by a first-order transfer function based on the design in Example 13-2. Design a P-type controller for the same open-loop crossover frequency as in Example 13-3 and for a phase margin of 60 degrees. Compare your results with those in Example 13-3.

13-6 In an actual system in which there are limits on the voltage and current that can be supplied, why and how does the initial steady-state operating point make a difference for large-signal disturbances?

13-7 Obtain the time response of the system designed in Example 13-2, in terms of the change in speed, for a step-change of the load-torque disturbance.

13-8 Obtain the time response of the system designed in Example 13-3, in terms of the change in position, for a step-change of the load-torque disturbance.

13-9 In the example system of Table 13-1, the maximum output voltage of the dc-dc converter is limited to 60 *V*. Assume that the current is limited to 8 *A* in magnitude. How do these two limits impact the response of the system to a large step-change in the reference value?

13-10 In Example 13-2, design the speed-loop controller, without the inner current loop, for the same crossover frequency and phase margin as in Example 13-2. Compare results with the system of Example 13-2.

Chapter 14

THYRISTOR CONVERTERS

14-1 INTRODUCTION

Historically, thyristor converters were used to perform tasks that are now performed by switch-mode converters discussed in previous chapters. Thyristor converters are now typically used in utility applications at very high power levels. In this chapter, we will examine the operating principles of thyristor-based converters.

14-2 Thyristors (SCRs)

Thyristors are a device that can be considered as a controlled diode. Like diodes, they are available in very large voltage and current ratings, making them attractive for use in applications at very high power levels.

Thyristors, shown by their symbol in Fig. 14-1a are sometimes referred to by their trade name of Silicon Controlled Rectifiers (SCRs). These are 4-layer (p-n-p-n) devices as shown in Fig. 14-1b. When a reverse ($v_{AK} < 0$) voltage is applied, the flow of current is blocked by the junctions pn1 and pn3. When a forward ($v_{AK} > 0$) polarity voltage is applied and the gate terminal is open, the flow of current is blocked by the junction pn2, and the thyristor is considered to be in a forward-blocking state. In this forward-blocking state, applying a small positive voltage to the gate with respect to the cathode for a short interval supplies a pulse of gate current i_G that latches the thyristor in its on state, and subsequently the gate-current pulse can be removed.

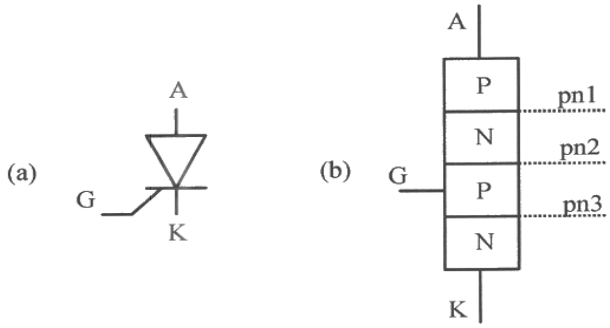
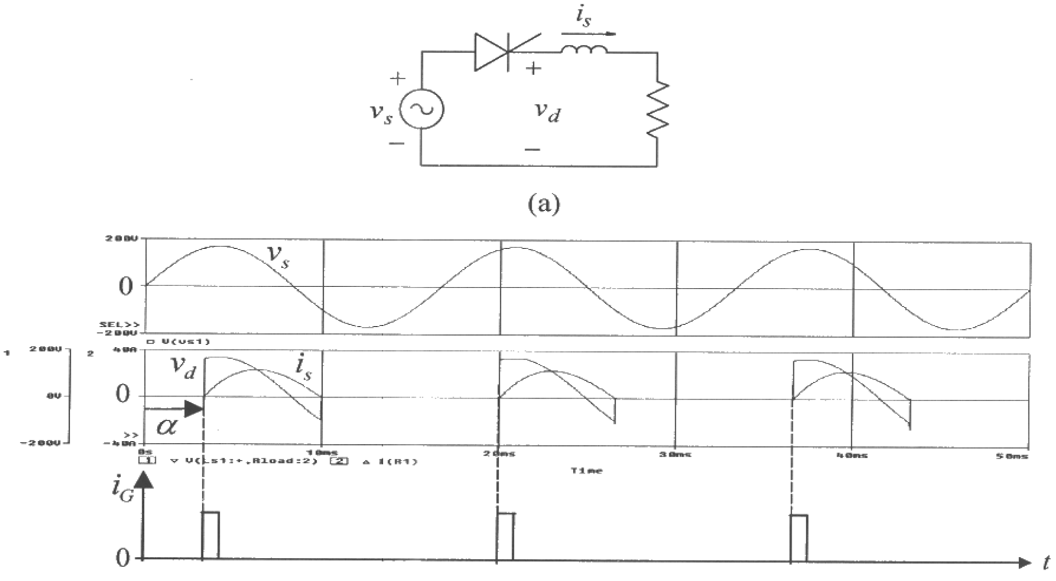


Figure 14-1 Thyristors.

The operation of thyristors is illustrated by means of a simple *R-L* circuit in Fig. 14-2a. At $\omega t = 0$, the positive-half-cycle of the input voltage begins, beyond which a forward voltage appears across the thyristor (anode A is positive with respect to cathode K), and if the thyristor were a diode, a current would begin to flow in this circuit. This instant $\omega t = 0$ in this circuit we will refer as the instant of natural conduction. With the thyristor forward blocking, the start of conduction can be controlled (delayed) with respect to $\omega t = 0$ by a delay angle α at which instant the gate-current pulse is applied. Once in the conducting state, the thyristor behaves like a diode with a very small voltage drop of the order of 1 to 2 volts across it (we will idealize it as zero), and the R-L load voltage v_d equals v_s, as shown in Fig. 14-2b.



(a)

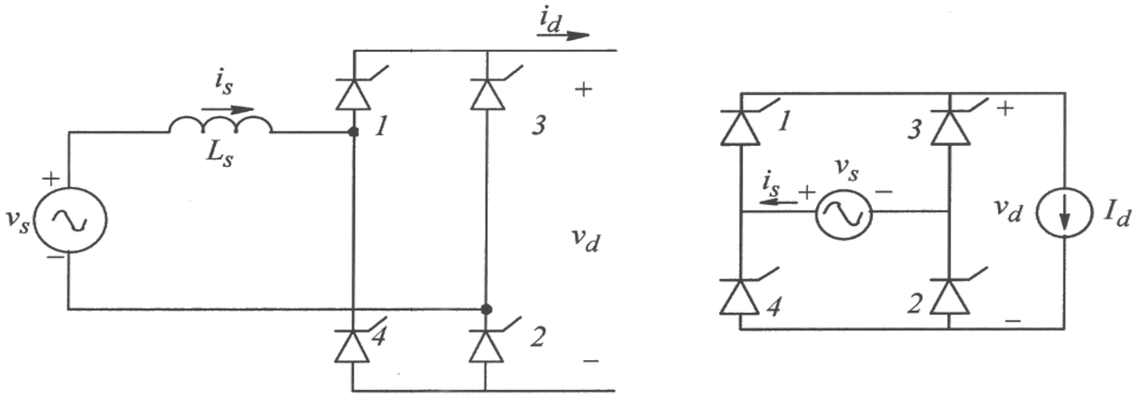
(b)

Figure 14-2 A simple thyristor circuit.

The current waveform in Fig. 14-2b show that due to the inductor, the current comes to zero sometime in the negative half-cycle of the input voltage. The current through the thyristor cannot reverse and remains zero for the remainder of the input voltage cycle. In the next voltage cycle, the current conduction again depends on the instant during the positive half-cycle at which the gate pulse is applied. By controlling the delay angle (or the phase control as it is often referred), we can control the average voltage v_d across the R-L load. This principle can be extended to the practical circuits discussed below.

14-3 Single-Phase, Phase-Controlled Thyristor Converters

Fig. 14-3a shows a commonly used Full-Bridge phase-controlled converter for controlled rectification of the single-phase utility voltage. To understand the operating principle, it is redrawn as in Fig. 14-3b, where the ac-side inductance L_s is ignored and the dc-side load is represented as drawing a constant current I_d. The waveforms are shown in Fig. 14-4.



(a) (b)

Figure 14-3 Full-Bridge, single-phase thyristor converter.

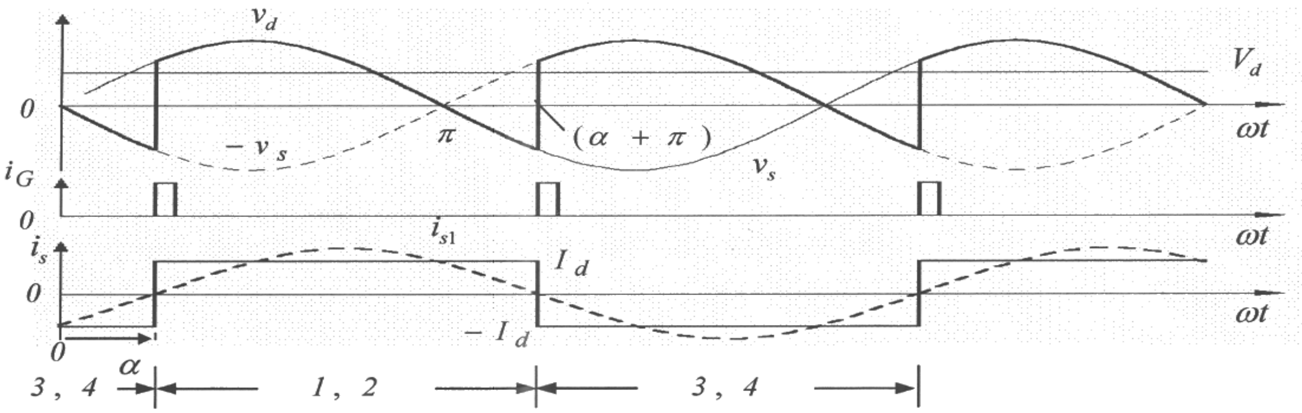


Figure 14-4 Single-phase thyristor converter waveforms.

Thyristors 1 and 2, and thyristors 3 and 4 are treated as two pairs, where each thyristor pair is supplied gate pulses delayed by an angle α with respect to its instant of natural conduction; $\omega t = 0^0$ for thyristors 1 and 2, and $\omega t = 180^0$ for thyristors 3 and 4, as shown in Fig. 14-4. In the positive half-cycle of the input voltage, thyristors 1 and 2 are forward-blocking until they are gated at $\omega t = \alpha$ when they immediately begin to conduct, and thyristors 3 and 4 become reverse-blocking. In this state,

$$v_d(t) = v_s(t) \quad \text{and} \quad i_s(t) = I_d \qquad \alpha < \omega t \le \alpha + \pi \qquad (14\text{-}1)$$

These relationships hold true until $\alpha + \pi$ in the negative half-cycle of the input voltage, when thyristors 3 and 4 are gated and begin conducting. In this state,

$$v_d(t) = -v_s(t) \quad \text{and} \quad i_s(t) = -I_d \qquad \alpha + \pi < \omega t \le \alpha + 2\pi \qquad (14\text{-}2)$$

which holds true for one half-cycle, until the next half-cycle begins with the gating of thyristors 1 and 2.

Assuming the input ac voltage to be sinusoidal, the average value V_d of the voltage across the dc-side of the converter can be obtained by averaging the $v_d(t)$ waveform in Fig. 14-4 over one half-cycle during $\alpha < \omega t \leq \alpha + \pi$:

$$V_d = \frac{1}{\pi} \int_{\alpha}^{\alpha+\pi} \hat{V}_s \sin \omega t \cdot d(\omega t) = \frac{2}{\pi} \hat{V}_s \cos \alpha \qquad (14\text{-}3)$$

On the ac-side, the input current i_s waveform is shifted by an angle α with respect to the input voltage as shown in Fig. 14-4, and the fundamental-frequency component $i_{s1}(t)$ has a peak value of

$$\hat{I}_{s1} = \frac{4}{\pi} I_d \qquad (14\text{-}4)$$

In terms of voltage and current peak values, the power drawn from the ac-side is

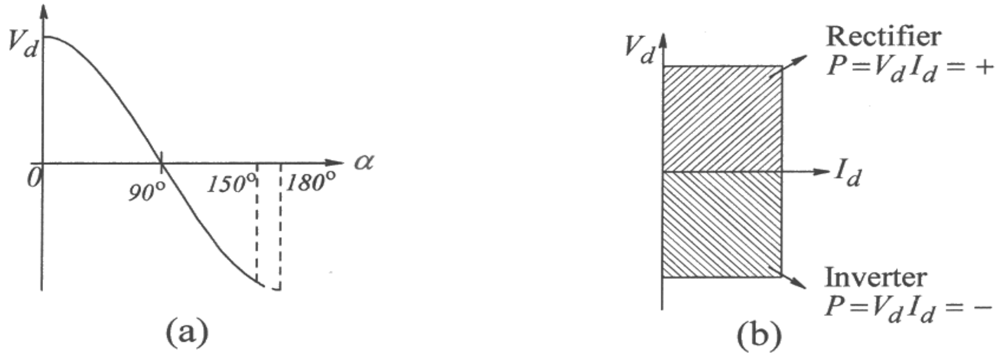
$$P = \frac{1}{2} \hat{V}_s \hat{I}_{s1} \cos \alpha \qquad (14\text{-}5)$$

Assuming no power loss in the thyristor converter, the input power equals the power to the dc-side of the converter. Using Eqs. 14-3 and 14-4, we can reconfirm the following relationship:

$$P = \frac{1}{2} \hat{V}_s \hat{I}_{s1} \cos \alpha = V_d I_d \qquad (14\text{-}6)$$

Power flow can be controlled by the delay angle α; increasing it toward 90^0 reduces the average dc-side voltage V_d while simultaneously shifting the input current $i_s(t)$ waveform farther away with respect to the input voltage waveform. The dc voltage as a function of α is plotted in Fig. 14-5a and the corresponding power direction is shown in Fig. 14-5b. The waveforms in Fig. 14-4 show that for the delay angle α in a range of 0^0 to 90^0, V_d has a positive value as plotted in Figs. 14-5a and b, and the converter operates as a rectifier, with power flowing from the ac-side to the dc-side.

Delaying the gating pulse such that α is greater than 90^0 in Fig. 14-4 makes V_d in Eq. 14-3 negative, and the converter operates as an inverter as shown in Fig. 14-5b, with power flowing from the dc-side to the ac-side. In practice, the upper limit on α in the inverter is below 180^0, for example 160^0 to avoid a phenomenon known as the commutation failure, where the current fails to commutate fully from the conducting thyristor pair to the next pair, prior to the instant beyond which the conducting pair keeps on conducting for another half-cycle. This commutation-failure phenomena is fully described in [1].

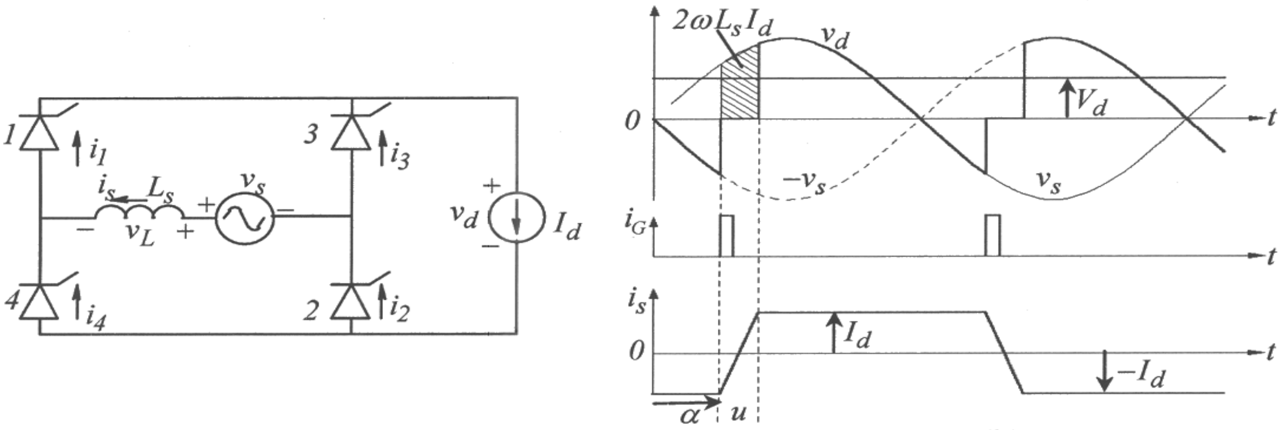


(a) (b)

Fig. 14-5 Effect of the delay angle α.

14-3-1 The Effect of L_s on Current Commutation

Previously, our assumption was that the ac-side inductance L_s equals zero. In the presence of this inductance, the input current takes a finite amount of time to reverse its direction, as the current "commutates" from one thyristor pair to the next.



(a) (b)

Figure 14-6 Effect of L_s on Current Commutation.

From basic principles, we know that changing the current through the inductor L_s in the circuit of Fig. 14-6a requires a finite amount of volt-seconds. The dc-side is still represented by a dc current I_d. The waveforms are shown in Fig. 14-6b, where thyristors 3 and 4 are conducting prior to $\omega t=\alpha$, and $i_s=-I_d$.

At $\omega t=\alpha$, thyristors 1 and 2, which have been forward blocking, are gated and hence they immediately begin to conduct. However, the current through them doesn't jump instantaneously as in the case of $L_s=0$ where i_s instantaneously changed from $(-I_d)$ to

$(+I_d)$. With a finite L_s, during a short interval called the commutation interval *u*, all thyristors conduct, applying v_s across L_s in Fig. 14-6a. The volt-radians needed to change the inductor current from $(-I_d)$ to $(+I_d)$ can be calculated by integrating the inductor voltage $v_L (= L_s \cdot di_s / dt)$ from α to $(\alpha + u)$, as follows:

$$\int_{\alpha}^{\alpha+u} v_L \, d(\omega t) = L_s \int_{\alpha}^{\alpha+u} \frac{di_s}{dt} d(\omega t) = \omega L_s \int_{-I_d}^{I_d} di_s = \omega L_s (2I_d) \qquad (14\text{-}7)$$

The above volt-radians are "lost" from the integral of the dc-side voltage waveform in Fig. 14-6b every half-cycle, as shown by the shaded area in Fig. 14-6b. Therefore, dividing the volt-radians in Eq. 14-7 by the π radians each half-cycle, the voltage drop in the dc-side voltage is

$$\Delta V_d = \frac{2}{\pi} \omega L_s I_d \qquad (14\text{-}8)$$

This voltage is lost from the dc-side average voltage in the presence of L_s. Therefore, the average voltage is smaller than that in Eq. 14-3:

$$V_d = \frac{2}{\pi} V_s \cos\alpha - \frac{2}{\pi} \omega L_s I_d \qquad (14\text{-}9)$$

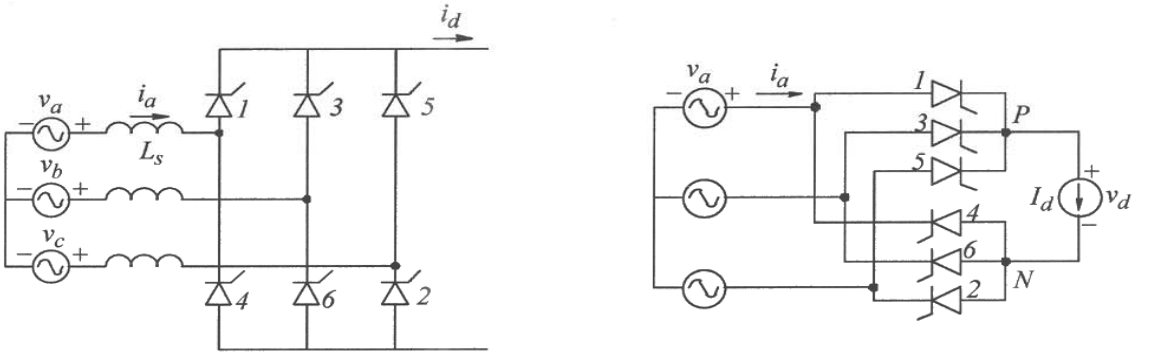
We should note that the voltage drop in the presence of L_s doesn't mean a power loss in L_s; it simply means a reduction in the voltage available on the dc-side.

14-4 THREE-PHASE, FULL-BRIDGE THYRISTOR CONVERTERS

Three-phase Full-Bridge converters use six thyristors, as shown in Fig. 14-7a. A simplified converter for initial analysis is shown in Fig. 14-7b, where the ac-side inductance L_s is assumed zero, thyristors are divided into a top group and a bottom group, similar to the three-phase diode rectifiers, and the dc-side is represented by a current source I_d.

The converter waveforms, where the delay angle α (measured with respect the instant at which phase voltage waveforms cross each other) is zero are similar to that in diode rectifiers discussed in Chapter 5 (see Figs. 5-11 and 5-12). The average dc voltage is as calculated in Eq. 5-23, where $\hat{V}_{LL}$ is the peak value of the ac input voltage:

$$V_{do} = \frac{1}{\pi/3} \int_{-\pi/6}^{\pi/6} \hat{V}_{LL} \cos\omega t \cdot d(\omega t) = \frac{3}{\pi} \hat{V}_{LL} \qquad (14\text{-}10)$$



(a) (b)

Figure 14-7 Three-phase Full-Bridge thyristor converter.

Delaying the gate pulses to the thyristors by an angle α measured with respect to their instants of natural conductions, the waveforms are shown in Fig. 14-8, where $L_s = 0$.

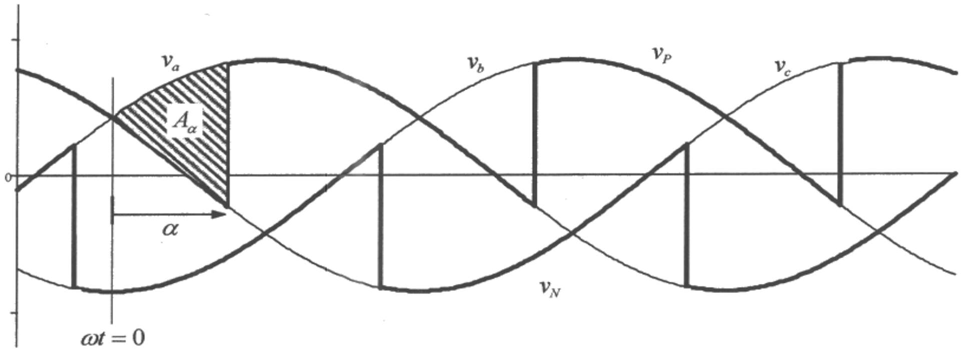


Figure 14-8 Waveforms with $L_s = 0$.

In the dc-side output voltage waveforms, the area A_α corresponds to "volt-radians loss" due to delaying the gate pulses by α every $\pi/3$ radian. Assuming the time-origin as shown in Fig. 14-8 at the instant at which the phase voltage waveforms cross, the line-line voltage v_{ac} waveform can be expressed as $\hat{V}_{LL} \sin \omega t$. Therefore from Fig. 14-8, the drop ΔV_α in the average dc-side voltage can be calculated as

$$\Delta V_\alpha = \frac{1}{\pi/3} \underbrace{\int_0^\alpha \hat{V}_{LL} \sin \omega t \cdot d(\omega t)}_{A_\alpha} = \frac{3}{\pi} \hat{V}_{LL} (1 - \cos \alpha) \tag{14-11}$$

14-4-1 Effect of L_s

As shown in the waveforms of Fig. 14-9, the average dc output voltage due to the presence of L_s is reduced by the area A_u every $\pi/3$ radian. During the commutation interval u, from α to $\alpha + u$, the instantaneous dc voltage is reduced due to the voltage drop across the inductance in series with the thyristor to which the current is commutating from 0 to $(+I_d)$. Using the procedure in Eq. 14-7 for single-phase converters,

$$A_u = \int_{\alpha}^{\alpha+u} v_L\, d(\omega t) = \omega L_s \int_{0}^{I_d} di_s = \omega L_s I_d \tag{14-12}$$

and therefore the voltage drop due to the presence of L_s is

$$\Delta V_u = \frac{A_u}{\pi/3} = \frac{3}{\pi}\omega L_s I_d \tag{14-13}$$

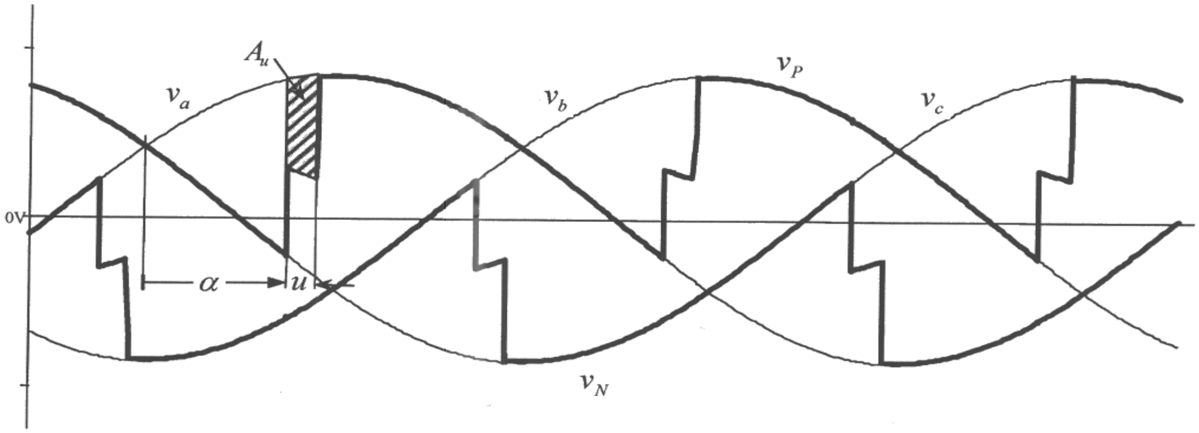


Figure 14-9 Waveforms with L_s.

Therefore, the dc-side output voltage can be written as

$$V_d = V_{do} - \Delta V_\alpha - \Delta V_u \tag{14-14}$$

Substituting results from Eqs. 14-10, 14-11, and 14-13 into Eq. 14-14

$$V_d = \frac{3}{\pi}\hat{V}_{LL}\cos\alpha - \frac{3}{\pi}\omega L_s I_d \tag{14-15}$$

Similar to single-phase converters, three-phase thyristor converters go into inverter mode with the delay angle α exceeding 90^0. In the inverter mode, the upper limit on α is less than 180^0 to avoid commutation failure, just like in single-phase converters. Further details on thyristor converters can be found in Reference [1].

14-5 Current-Link Systems

Thyristors are available in very large current and voltage ratings of several kAs and several kVs that can be connected in series. In addition, thyristor converters can block voltages of both polarities but conduct current only in the forward direction. This capability has led to the interface realized by thyristor-converters with a dc-current link in the middle, as shown in Fig. 14-10. Unlike in voltage-link systems, the transfer of power in current-link systems can be reversed in direction by reversing the voltage polarity of the dc-link. This structure is used at very high power levels, at tens of hundreds of MWs, for example in High Voltage DC Transmission (HVDC).

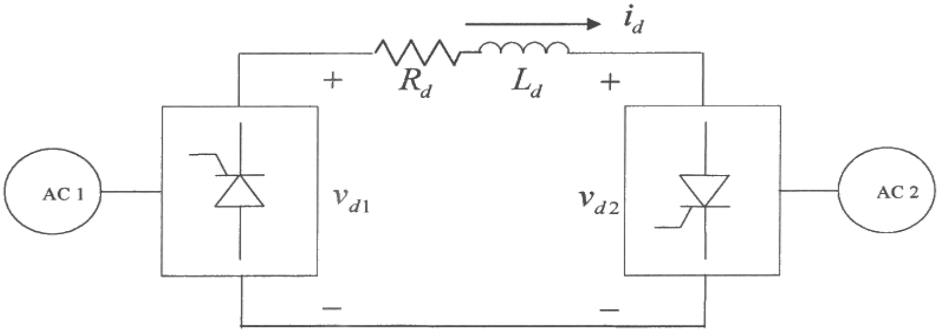


Figure 14-10 Block diagram of current-link systems.

Thyristors in these two converters shown in Fig. 14-10 are connected to allow the flow of current in the dc-link by thyristors in converter 1 pointing up, and the thyristors in converter 2 connected to point downward. In Fig. 14-10, subscripts 1 and 2 refer to systems 1 and 2 and R_d is the resistance of the dc-link inductance. Assuming each converter a six-pulse thyristor converter as discussed previously,

$$V_{d1} = \frac{3}{\pi}\hat{V}_{LL1}\cos\alpha_1 - \frac{3}{\pi}\omega L_{s1} I_d \tag{14-16}$$

$$V_{d2} = \frac{3}{\pi}\hat{V}_{LL2}\cos\alpha_2 - \frac{3}{\pi}\omega L_{s2} I_d \tag{14-17}$$

By controlling the delay angles α_1 and α_2 in a range of 0° to 180° (practically, this value is limited to approximately 150°), the average voltage and the average current in the system of Fig. 14-10 can be controlled, where current flow through the dc-link can be expressed as

$$I_d = \frac{V_{d1} + V_{d2}}{R_d} \tag{14-18}$$

where the dc-link resistance R_d is generally very small. In such a system, for the power flow from system 1 to system 2, V_{d2} is made negative by controlling α_2 such that it operates as an inverter and establishes the voltage of the dc-link. The converter 1 is operated as a rectifier at a delay angle α_1 such that it controls the current in the dc-link. The converse is true for these two converters if the power is to flow from system 2 to system 1.

The above discussion of current-link systems shows the operating principle behind HVDC transmission systems discussed in the next chapter, where using transformers, six-pulse thyristor converters are connected in series on the dc-side and in parallel on the ac-side to yield higher effective pulse number.

REFERENCE

1. N. Mohan, T. M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, Wiley & Sons, New York, 2003.

PROBLEMS

Single-Phase Thyristor Converters

In a single-phase thyristor converter, $V_s = 120V(rms)$ at $60\,Hz$, and $L_s = 3mH$. The delay angle $\alpha = 30^0$. This converter is supplying $1kW$ of power. The dc-side current i_d can be assumed purely dc.

14-1 Calculate the commutation angle u.

14-2 Draw the waveforms for the converter variables.

14-3 Calculate the DPF, %THD in the input current, and the PF of operation of this converter.

Three-Phase Thyristor Converters

In a three-phase thyristor converter, $V_{LL} = 460V(rms)$ at $60\,Hz$, and $L_s = 5mH$. The delay angle $\alpha = 30^0$. This converter is supplying $5kW$ of power. The dc-side current i_d can be assumed purely dc.

14-4 Calculate the commutation angle u.

14-5 Draw the waveforms for the converter variables.

14-6 Calculate the DPF, %THD in the input current, and the PF of operation of this converter.

Chapter 15

UTILITY APPLICATIONS OF POWER ELECTRONICS

15-1 INTRODUCTION

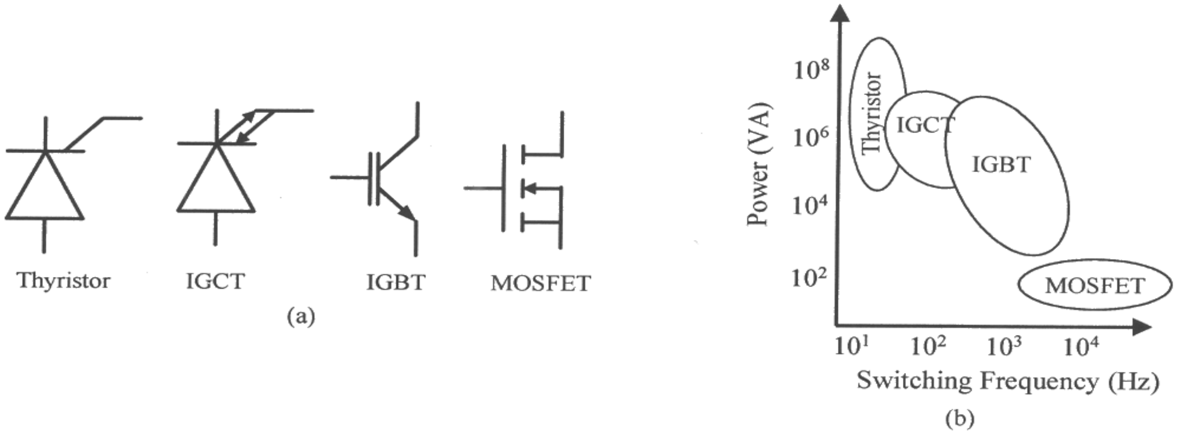
Power electronics applications in utility systems are growing very rapidly, which promise to change the landscape of future power systems in terms of generation, operation and control. The goal of this chapter is to briefly present an overview of these applications to prepare students for new challenges in the deregulated utility environment and to motivate them to take further courses in this field, where a separate advanced-level graduate course is designed, for example at the University of Minnesota, to discuss these topics in detail.

In discussing these applications, we will observe that the power electronic converters are the same or modifications of those that we have already discussed in earlier chapters. Therefore, within the scope of this book, it will suffice to discuss these applications in terms of the block diagrams of various converters. These utility applications of power electronics can be categorized as follows:

- Distributed Generation (DG)
    - Renewable Resources (Wind, Photovoltaic, etc.)
    - Fuel Cells and Micro-Turbines
    - Storage - Batteries, Super-conducting Magnetic Storage, Flywheels
- Power Electronic Loads - Adjustable Speed Drives
- Power Quality Solutions
    - Dual Feeders
    - Uninterruptible Power Supplies
    - Dynamic Voltage Restorers
- Transmission and Distribution (T&D)
    - High Voltage DC (HVDC) and HVDC-Light
    - Flexible AC Transmission (FACTS)
        - Shunt Compensation
        - Series Compensation
        - Static Phase Angle Control and Unified Power Flow Controllers

15-2 POWER SEMICONDUCTOR DEVICES AND THEIR CAPABILITIES [1]

Fig. 15-1a shows the commonly used symbols of power devices. The power handling capabilities and switching speeds of these devices are indicated in Fig. 15-1b. All these devices allow current flow only in their forward direction (the intrinsic anti-parallel diode of MOSFETs can be explained separately). Transistors (intrinsically or by design) can block only the forward polarity voltage, whereas thyristors can block both forward and reverse polarity voltages. Diodes are uncontrolled devices, which conduct current in the forward direction and block a reverse voltage. At very high power levels, integrated-gate controlled thyristors (IGCTs), which have evolved from the gate-turn-off thyristors, are used. Thyristors are semi-controlled devices that can switch-on at the desired instant in their forward-blocking state, but cannot be switched off from their gate and hence rely on the circuit in which they are connected to switch them off. However, thyristors are available in very large voltage and current ratings.



(a)

(b)

Figure 15-1 Power semiconductor devices.

15-3 CATEGORIZING POWER ELECTRONIC SYSTEMS

In a very broad sense, the role of power electronics in these power system applications can be categorized as follows:

15-3-1 Solid-State Switches

By connecting two thyristors in anti-parallel (back-to-back) as shown in Fig. 15-2, it is possible to realize a solid-state switch which can conduct current in both directions, and turn-on or turn-off in an ac circuit with a delay of no more than one-half the line-frequency cycle. Such switches are needed for applications such as dual feeders, shunt-compensation for injecting reactive power at a bus for voltage control, and series-compensation of transmission lines.

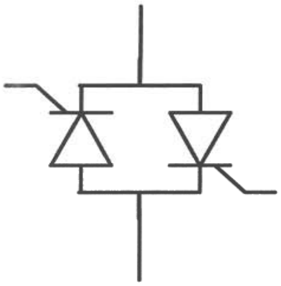


Figure 15-2 Back-to-back thyristors to act as a solid-state switch.

15-3-2 Converters as an Interface

Power electronic converters provide the needed interface between the electrical source, often the utility, and the load, as shown in Fig. 15-3. The electrical source and the electrical load can, and often do, differ in frequency, voltage amplitudes and the number of phases. The power electronics interface allows the transfer of power from the source to the load in the most energy efficient manner, in which it is possible for the source and load to reverse roles. These interfaces can be classified as below.

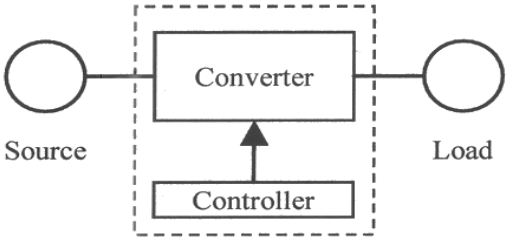


Figure 15-3 Power electronics interface.

15-3-2-1 Voltage-Link Systems

The semiconductor devices such as transistors of various types and diodes can only block forward-polarity voltages. These devices with only unipolar voltage-blocking capability have led to the structure with two converters, where the dc ports of these two converters are connected to each other with a parallel capacitor forming a dc-link in Fig. 15-4, across which the voltage polarity does not reverse, thus allowing unipolar voltage-handling transistors to be used within these converters. The transfer of power can be reversed in direction by reversing the direction of currents associated with the dc-link system.

Voltage-link converters consist of switching power-poles as the building blocks, which can synthesize the desired output by means of Pulse Width Modulation (PWM) and have the bi-directional power flow capability. Such switching power-poles can be modeled by means of an ideal transformer with a controllable turns-ratio, as discussed in Chapter 12.

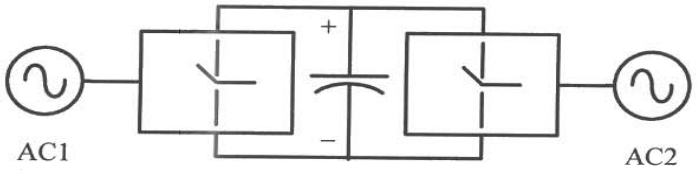


Fig. 15-4 Block diagram of the voltage-link systems.

15-3-2-2 Current-Link Systems

Thyristors can block voltages of both polarities but conduct current only in the forward direction. This capability has led to the interface realized by thyristor-converters with a dc-current link in the middle, as shown in Fig. 15-5. The transfer of power can be reversed in direction by reversing the voltage polarity of the dc-link, but the currents in the link remain in the same direction. This structure is used at very high power levels, at tens of hundreds of MWs, for example in High Voltage DC Transmission (HVDC).

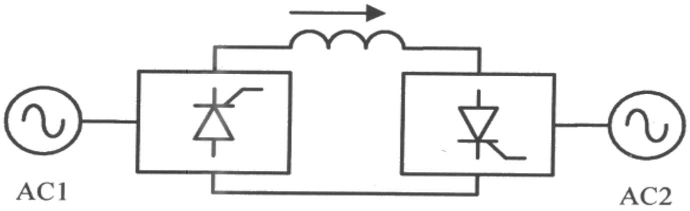


Figure 15-5 Block diagram of the current-link systems.

In the following sections, various utility applications and the role of power electronics in them are examined further.

15-4 DISTRIBUTED GENERATION (DG) APPLICATIONS

Distributed generation, shown in Fig. 15-6 from the control perspective, promises to change the landscape of how power systems of the future will be operated and controlled. These generators may have decentralized (local) control, in addition to a central supervisory control.

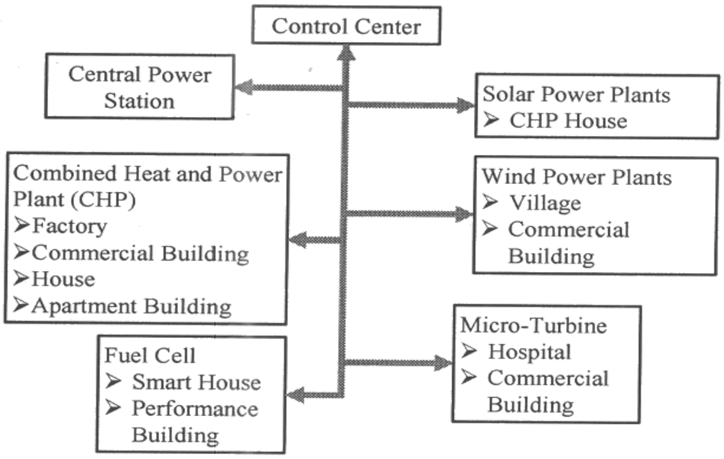

Control Center
Central Power Station
Solar Power Plants
➢ CHP House
Combined Heat and Power Plant (CHP)
➢Factory
➢Commercial Building
➢House
➢Apartment Building
Wind Power Plants
➢ Village
➢ Commercial Building
Micro-Turbine
➢ Hospital
➢ Commercial Building
Fuel Cell
➢ Smart House
➢ Performance Building

Figure 15-6 Distributed Generation (DG) systems.

There is a move away from large central power plants towards distributed generation due to environmental and economic reasons. Renewable resources such as wind and photovoltaic systems are growing in their popularity. There are proposals to place highly efficient small-scale power plants, based on fuel cells and micro-turbines, near load centers to simultaneously avoid transmission congestion and line losses. Many of distributed generation systems are discussed below.

15-4-1 Wind-Electric Systems

Wind energy is the fastest growing energy resource in the world. In 2002, the amount of installed wind energy in the world reached nearly 30,000 MW, and the installed wind energy in the U.S. alone increased by 66% in 2001. This remarkable growth is spurred by a combination of environmental concerns, decreasing costs of wind electric systems, and financial incentives for wind park developers.

There are many schemes for harnessing wind energy, out of which those using doubly-fed induction generators are enjoying increased popularity. As shown in Fig. 15-7, in this system, the stator which produces most of the power is connected directly to the grid. The rotor windings are accessible through slip-rings and brushes to a power electronic converter system, which supplies the rotor current. By injecting currents into the rotor, the machine can be made to act like a generator at both sub-synchronous and super-synchronous speeds. The converter rating is about 15% of the rated power, for example, in the 750 kW doubly-fed induction machines used in the southwestern Minnesota for wind-electric systems, only 150 kW flows through the rotor, and the rest through the stator. Injecting current into the rotor provides control over the real and the reactive power (leading or lagging).

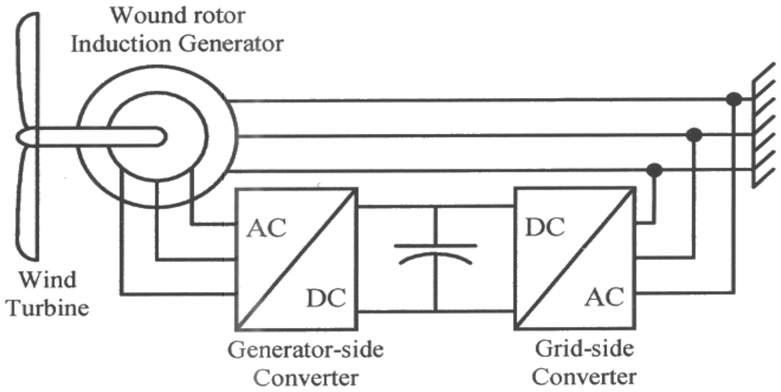


Figure 15-7 Doubly-fed induction generators for wind-electric systems.

15-4-2 Photovoltaic (PV) Systems

Photovoltaic systems are the ultimate in distributed generation and have even a greater potential than the wind-electric systems. In 1997, PV systems surpassed the 500 MW threshold in worldwide installation, and annual global sales of $1 billion. A few years back, the Clinton administration announced the 'million solar roof initiative', emphasizing the growing importance of PV systems.

In PV systems, the PV arrays (typically four of them connected in series) provide a voltage of 52-V to 90-V DC, which the power electronic system, as shown in Fig. 15-8, converts to 120V/60Hz sinusoidal voltage suitable for interfacing with the single-phase utility. PV modules are still very expensive, as much as $1,500 for only a 300 W peak output. Such PV modules can be connected in parallel for higher output capacity. Presently there is not much economy of scale in the PV modules, making it prudent to invest in steps.

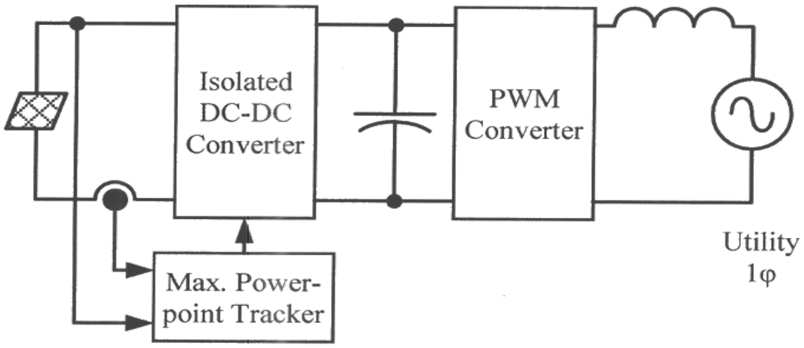


Figure 15-8 Photovoltaic systems.

15-4-3 Fuel Cell Systems

Lately, there has been a great deal of interest in, and effort being devoted to fuel cell systems. The reason has to do with their efficiency, which can be as high as 60 percent. The input to the fuel cell can be natural gas or gasoline and the output is a dc voltage. The need for power electronics converters to interface with the utility is the same in the fuel-cell systems as that for the photovoltaic systems.

15-4-4 Micro-Turbines

These use highly efficient aircraft engines, for example to produce peak power when it is needed, with the natural gas as the input fuel. To improve efficiency, the turbine speed should be allowed to vary based on loading. This will cause the frequency of the generated output to vary, requiring a power-electronic interface as that in adjustable-speed drives.

15-4-5 Energy Storage Systems

Although not a primary source of energy, storage plants offer the benefit of load-leveling and peak-shaving in power systems, because of the diurnal nature of electricity usage. Energy is stored, usually at night when the load demand is low, and supplied back during the peak-load periods. It is possible to store energy in lead-acid batteries (other exotic high-temperature batteries are being developed), in Super-conducting Magnetic Energy Storage (SMES) coils and in the inertia of flywheels. All these systems need power electronics interface, where the interface for the flywheel storage is shown in Fig. 15-9.

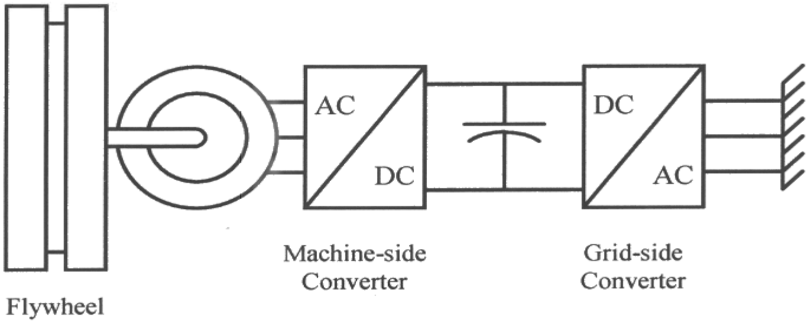


Figure 15-9 Flywheel storage system.

15-5 POWER ELECTRONIC LOADS

As discussed in Chapter 1, power electronics is playing a significant role in energy conservation, for example, as users discover the benefits of reduced energy consumption and better process control by operating electric drives at adjustable speeds. An adjustable-speed drive (ASD) is shown in Fig. 15-10 in a block diagram form. Power electronic loads of this type often use an interface with the utility that results in distorted line currents. These currents result in distorted voltage waveforms, affecting the neighboring loads. However, it is possible to design the utility interface (often called the power-factor-corrected front-end) that allows sinusoidal currents to be drawn from the grid. With the proliferation of power electronics loads, standards are being enforced that limit the amount of distortion in currents drawn.

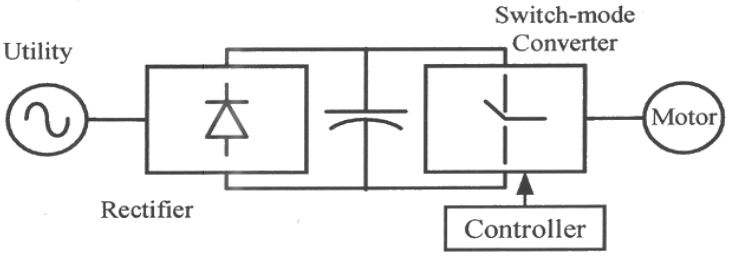


Figure 15-10 Adjustable-speed drive.

15-6 POWER QUALITY SOLUTIONS

Poor quality of power can imply any of the following: distorted voltage waveforms, unbalances, swells and sags in voltage and power outages, etc. This problem is exacerbated in a deregulated environment where utilities are forced to operate at marginal profits, resulting in inadequate maintenance of equipment. In this section, we will also see that power electronics can solve many of the power quality problems.

15-6-1 Dual Feeders

The continuity of service can be enhanced by dual power feeders to the load, where one acts as a backup to the other that is supplying the load as shown in Fig. 15-11. Using back-to-back connected thyristors, acting as a solid-state switch, it is possible to switch the load quickly, without interruption, from the main feeder to the backup feeder and back.

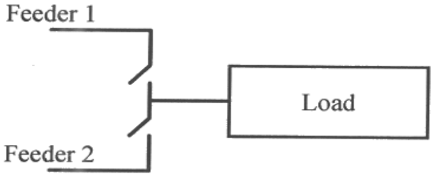


Figure 15-11 Dual-feeders.

15-6-2 Uninterruptible Power Supplies

Power outages, even for a few cycles, can be very disruptive to critical loads. To provide immunity from such outages, power-electronics-based uninterruptible power supplies (UPS) shown in Fig. 15-12 can be used, where the energy storage can be by means of batteries, SMES, flywheels or super-capacitors.

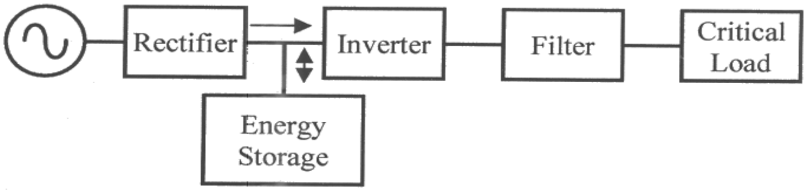


Figure 15-12 Uninterruptible power supplies.

15-6-3 Dynamic Voltage Restorers

Dynamic Voltage Restorers (DVR), shown in Fig. 15-13, can compensate for voltage sags or swells by injecting a voltage v_{inj} in series with that supplied by the utility.

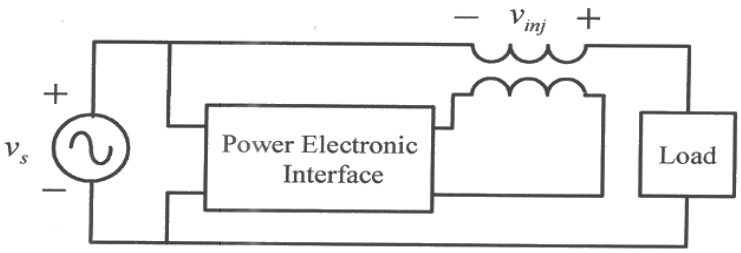


Figure 15-13 Dynamic voltage restorers.

15-7 TRANSMISSION AND DISTRIBUTION (T&D) APPLICATIONS

In the past, utilities operated as monopolies, where users had little or no option in selecting whom they can purchase power from. The recent trend, which seems irreversible in spite of recent setbacks, is to deregulate where utilities must compete to sell power on an open market and the customers have a choice of selecting their power provider. In such an environment, utilities that were vertically integrated are now forced to split into generation companies that produce power, and transmission-line operators that maintain the transmission and distribution network for a fee.

In this deregulated environment, it is highly desirable to have the capability to dictate the flow of power on designated power lines, avoiding overloading of transmission lines and excessive power losses in them. In this section, we will look at some such options.

15-7-1 High Voltage DC (HVDC) and Medium Voltage DC (MVDC) Transmission

Direct current (DC) transmission represents the ultimate in flexibility, isolating two interconnected ac systems from the requirement of operating in synchronism or even at the same frequency. High voltage DC (HVDC) systems using thyristor-based converters have now been in operation for several decades. Lately, such systems at medium voltages have been proposed. Both of these types of systems are discussed below.

15-7-1-1 High Voltage DC (HVDC) Transmission

Fig. 15-14 shows the block diagram of a HVDC transmission system, where power is transmitted over dc lines at high voltages in excess of 500 kV. First, the voltages in ac system 1 at the sending end are stepped up by means of a transformer. These voltages are rectified into dc by means of a thyristor-based converter, where the ac line voltages provide the commutation of current within the converter, such that ac currents drawn from system 1 turn into dc current on the other side of the converter. These currents are transmitted over the dc line where additional series inductance is added to ensure that the dc current is smooth, free of ripple as much as possible. At the receiving end, there are thyristor-based converters, which convert the dc current into ac currents and injects them into the ac system 2, through a step-down transformer. The roles of the sending and the receiving ends can be reversed by reversing the voltage polarity in the dc system.

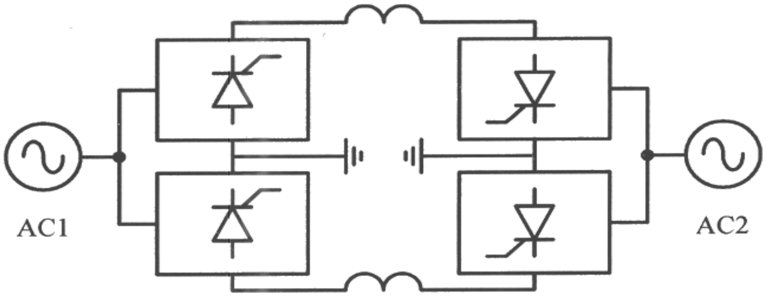


Figure 15-14 HVDC system block diagram (transformers are not shown).

At very high power levels in excess of 1,000 MW, use of thyristors, at least for now, represents the only reasonable choice.

15-7-1-2 Medium Voltage DC (MVDC) Transmission

At lower power levels, there are proposals to use medium voltages, in which case the block diagram of the system is as shown in Fig. 15-15. In such a system, the direction of power flow is reversed by changing the direction of current in the dc line.

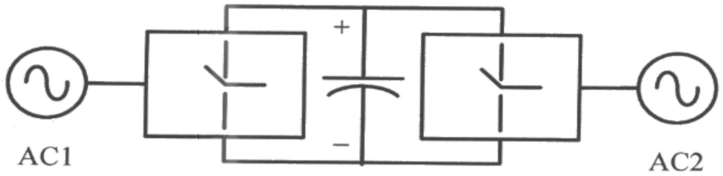


Figure 15-15 Block diagram for medium-voltage dc transmission systems.

15-7-2 Flexible AC Transmission Systems (FACTS) [2]

DC transmission systems discussed earlier are an excellent choice where large amount of power needs to be transmitted over long distances, or if the system stability is a serious issue. In existing ac transmission networks, limitation on constructing new power lines and their cost has led to other ways to increase power transmission capability without sacrificing the stability margin. These techniques may also help in directing the power flow to designated lines.

Power flow on a transmission line connecting two ac systems in Fig. 15-16 is given as

$$P = \frac{E_1 E_2}{X} \sin\delta \tag{15-1}$$

where E_1 and E_2 are the magnitudes of voltages at the two ends of the transmission line, X is the line reactance and δ is the angle between the two bus voltages.

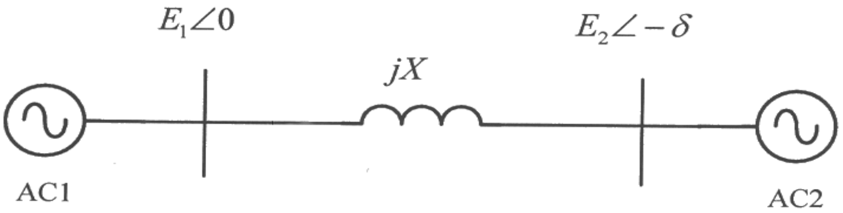


Figure 15-16 Power flow on a transmission line.

Eq. 15-1 shows that the power flow on a transmission line depends on three quantities: (1) the voltage magnitude E, (2) the line reactance X, and (3) the power angle δ. Various devices which are based on rapidly controlling one or more of the above three quantities are discussed in the following sections:

15-7-2-1 Shunt-Connected Devices to Control the Bus Voltage Magnitude E

The reactive power compensation is very important and may even be necessary at high loadings to avoid voltage collapse. Shunt-connected devices can draw or supply reactive power from a bus, thus controlling the bus voltage, albeit in a limited range, based on the internal system reactance. Various forms of such devices are being used in different combinations. These include Thyristor-Controlled Reactors (TCR) shown in Fig. 15-17a, and Thyristor-Switched Capacitors (TSC) shown in Fig. 15-17b for Static Var Compensation (SVC). The advanced Static Var Compensator (STATCOM) shown in Fig. 15-17c can draw or supply reactive power.

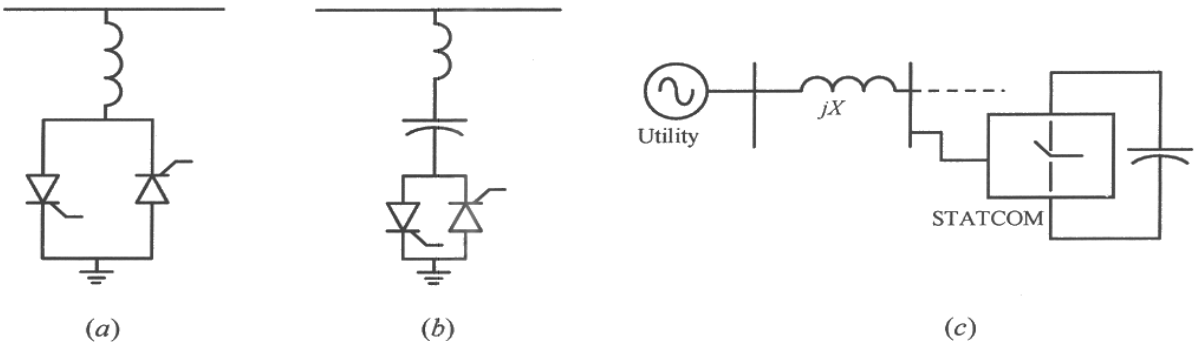


Figure 15-17 Shunt-connected devices for voltage control.

Shunt-compensation devices have the following limitations for controlling the flow of active power:

1. A large amount of reactive power compensation, depending on the system internal reactance, may be required to change the voltage magnitude. Of course, the voltage can only be changed in a limited range (utilities try to maintain bus voltages at their nominal values), which has a limited effect on the power transfer given by Eq. 15-1.
2. Most transmission systems consist of parallel paths or loops. Therefore, changing the voltage magnitude at a given bus changes the loading of all the lines connected to that bus, and there is no way to dictate the desired change of power flow on a given line.

15-7-2-2 Series-Connected Devices to Control the Effective Series Reactance X

These devices, connected in series with a transmission line, partially neutralize (or add to) the transmission line reactance. Therefore, they change the effective value of X in Eq. 15-1, thus allowing the active power flow P to be controlled. Various forms of such devices have been used. These include the Thyristor-Controlled Series Capacitor (TCSC) shown in Fig. 15-18.

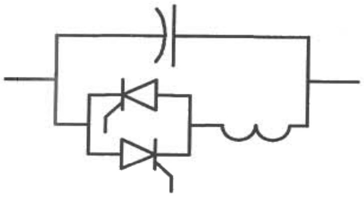


Figure 15-18 Thyristor-controlled series capacitor.

15-7-2-3 Static Phase Angle Control and Unified Power Flow Controller (UPFC)

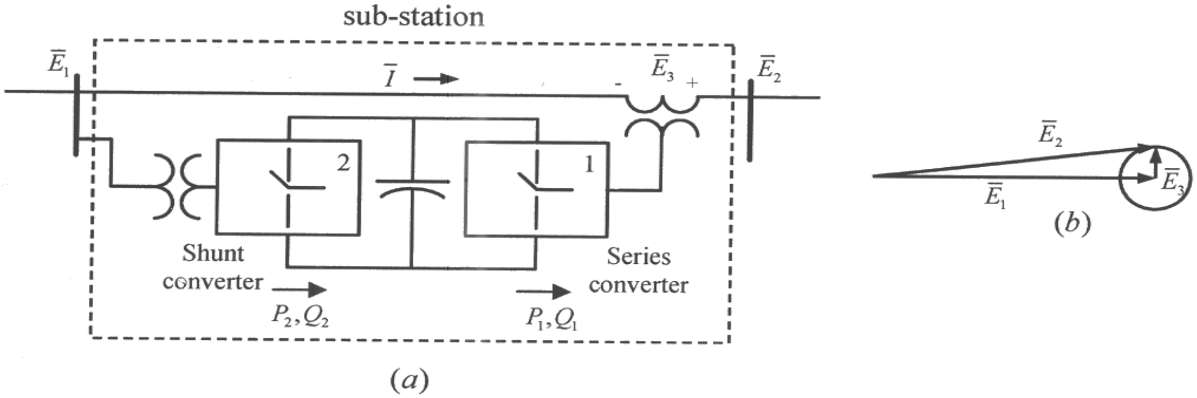
Based on Eq. 15-1, a device connected at a bus in a substation, as shown in Fig. 15-19a, can influence power flow in three ways by:

1. controlling the voltage magnitude E
2. changing the line reactance X, and/or
3. changing the power angle δ.

Such a device called the Unified Power Flow Controller (UPFC) can affect power flow in any combination of the ways listed above. The block diagram of a UPFC is shown in Fig. 15-19a at one side of the transmission line. It consists of two voltage-source switch-mode converters. The first converter injects a voltage $\overline{E}_3$ in series with the phase voltage such that

$$\overline{E}_1 + \overline{E}_3 = \overline{E}_2 \tag{15-2}$$

Therefore, by controlling the magnitude and the phase of the injected voltage $\overline{E}_3$ within the circle shown in Fig. 15-19b, the magnitude and the phase of the bus voltage $\overline{E}_2$ can be controlled. If a component of the injected voltage $\overline{E}_3$ is made to be 90 degrees out-of-phase, for example leading with respect to the current phasor $\overline{I}$, then the transmission line reactance X is partially compensated.



sub-station
$\overline{E}_1$
$\overline{I}$
$\overline{E}_3$
-
+
$\overline{E}_2$
2
1
Shunt converter
Series converter
P_2, Q_2
P_1, Q_1
(a)
$\overline{E}_2$
$\overline{E}_1$
$\overline{E}_3$
(b)

Figure 15-19 UPFC.

The second converter in a UPFC is needed for the following reason: since converter 1 injects a series voltage $\overline{E}_3$, it delivers real power P_1, and the reactive power Q_1 to the transmission line (where P_1 and Q_1 can be either positive or negative):

$$P_1 = 3\,\mathrm{Re}(\overline{E}_3 \overline{I}^*) \tag{15-3}$$

$$Q_1 = 3\,\mathrm{Im}(\overline{E}_3 \overline{I}^*) \tag{15-4}$$

Since there is no steady state energy storage capability within UPFC, the power P_2 into converter 2 must equal P_1 if the losses are ignored:

$$P_2 = P_1 \tag{15-5}$$

However, the reactive power Q_2 bears no relation to Q_1, and can be independently controlled within the voltage and current ratings of the converter 2:

$$Q_2 \neq Q_1 \tag{15-6}$$

By controlling Q_2 to control the magnitude of the bus voltage $\overline{E}_1$, UPFC provides the same functionality as that of an advanced static var compensator STATCOM.

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PROBLEMS

15-1 Show the details and the average representation of converters in Fig. 15-7 for a wind-electric system.

15-2 Show the details and the average representation of converters in Fig. 15-8 for a photovoltaic system.

15-3 Show the details and the average representation of converters in Fig. 15-9 for a flywheel storage system.

15-4 Show the details and the average representation of converters in Fig. 15-10 for an adjustable-speed drive.

15-5 Show the details and the average representation of converters in Fig. 15-12 for a UPS.

15-6 Show the details and the average representation of converters in Fig. 15-13 for a DVR.

15-7 Show the details and the average representation of converters in Fig. 15-14 for an HVDC transmission system.

15-8 Show the details and the average representation of converters in Fig. 15-15 for an MVDC transmission system.

15-9 Show the details and the average representation of converter in Fig. 15-17c for a STATCOM.

15-10 Show the details and the average representation of converters in Fig. 15-19a for a UPFC system.

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